## 附件1

# 浙江工程师学院(浙江大学工程师学院) 同行专家业内评价意见书

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浙江工程师学院(浙江大学工程师学院)制 2025年03月13日

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四、同行专家业内评价意见书编号由工程师学院填写 ,编号规则为:年份4位+申报工程师职称专业类别(领域)4 位+流水号3位,共11位。

### 一、个人申报

# (一)基本情况【围绕《浙江工程师学院(浙江大学工程师学院)工程类专业学位研究生工程师职称评审参考指标》,结合该专业类别(领域)工程师职称评审相关标准,举例说明】

#### 1. 对本专业基础理论知识和专业技术知识掌握情况(不少于200字)

经过本次专业实践,在理论知识层面上,有效提升了我在硬件电路、功率模块、结温监测等领域的知识掌握程度,包括许多结温监测领域现存的技术痛点,是通过与公司的资深工程师讨论分析后,才能认识到的,目前实验室内的结温检测技术其实已经有许多发展,在热敏电阻、光学检测、热网络建模、热敏电参数法都有许多论文或专利发表,但通过本次专业实践,经过与工程师们的讨论,我才发现现有结温检测技术推广的痛点,也帮助我在确立毕设题目时选取更贴近工程上更有实际应用价值的选题。

#### 2. 工程实践的经历(不少于200字)

在能力提升层面上,经过本次专业实践的锻炼,对于我作为一位硬件工程师的能力有了全方位的提升,平时日常实践工作中,经常会有需要调试电路、焊接电路板、利用AD绘制原理图与PCB、利用串口助手进行单片机调试的机会,经过一年的实践时间,我对以上提到的实验技能有了极大的提升,特别是在公司工程师们的教导下,学习到了很多工程上实用的实验技巧,很多都是难以单纯通过在实验室里开展实验学到的技能。

在素质养成方面,在公司实践的一年里,我不仅只从身边的同事身上学到了专业知识和实验技能,也学习到了许多未来工作时很重要的能力,包括但不限于完整的工作流,一个电路设计从需求分析、需求拆解,再到电路设计、电路仿真、PCB

Layout、电路调试、各类测试,公司的工程师们都有非常详尽且科学的流程,按照设计好的流程进行硬件开发工作,可以有效地降低开发后电路板的故障可能,也可以有效的优化整个设计的流程,减少因为规划不合理造成的时间浪费。这都是我认为在未来工作中会有很大价值的非专业技能,也只有通过这样的专业实践的过程才可以学到这些技能。除此之外,在公司也有许多与不同部门同事沟通、讨论与学习的机会,比如有机会可以和Layout部门的同事交流功率回路的PCB布局、高速信号的布线规则,也有机会与软件部门的同事沟通单片机代码的修改,一起来优化控制策略的性能,当然也有机会与公司内相当有经验的各位优秀工程师们学习到很多行业内的信息与经验,这对于我未来的实验工作包括进入职场后的发展都有很大的帮助。

#### 3. 在实际工作中综合运用所学知识解决复杂工程问题的案例(不少于1000字)

针对IGBT结温监测中的温敏电参数法,基于大电流下饱和压降法中存在的连接件误差问题,提出了一种基于IGBT饱和压降拐点现象的IGBT大电流下等效压降结温检测方法,该方法可以从理论层面上消除IGBT饱和压降测量值中连接件阻抗所造成的误差,有效提高IGBT在线结温监测的精度;同时该方法有效的避免了常见的IGBT饱和压降测量方法中由于拐点电压附近结温灵敏度较低造成的检测精度下降问题,可以保证IGBT在更大的工况范围下,保持良好的结温检测精度;并且该结温检测方案相比于常见的IGBT大电流下饱和压降方案只增加了计算环节,未增加硬件部分或实验步骤,有效的保证了结温监测的简便性,保持了IGBT大电流下饱和压降结温检测法的低侵入性。大电流下饱和压降是在IGBT正常工作过程中的开通饱和状态下,进行饱和压降的测量,该电参数是目前研究最广泛,也是应用最全面的温敏电参数,其优势在于灵敏度较高,线性度好,对系统现有工作模式影响小,外设电路简单。但由于对其研究相对其他温敏电参数更为深入,该电参数的缺陷也相对较多,首先是IGBT模块老化会造成标定的数据无法契合真实的工况,同时该电参数存在温度系数拐点的问题,在一定电流等级以下,结温与饱和压降呈负温度系数,而在一定温度以上,呈正温度系数。同时还存在器

件之间参数的一致性,导致应用中必须通过对每一个IGBT模块都进行结温数据标定,才可以实现结温的精确反推。综上所述,虽然大电流下饱和压降法的缺点很多,但其依然是目前应用最广泛,且最具潜力的IGBT在线结温检测电参数。 学位论文定题为IGBT的智能驱动与状态监测,而本次专业实践当中核心的工作内容就包括状态监测里非常重要的结温监测技术,根据电力电子系统的可靠性调查研究,变流系统中最重要并且也是最容易失效的部分就是半导体器件,约占总失效比的34%,而半导体器件中IGBT

态监测里非常重要的结温监测技术,根据电力电子系统的可靠性调查研究,变流系统中最重要并且也是最容易失效的部分就是半导体器件,约占总失效比的34%,而半导体器件中IGBT 具有开关频率较高、耐压高、通流能力强等优势,现已成为目前变流器中使用最广泛的功率半导体器件。而近60%的器件失效是由温度引起的,在正常工作温度范围内,温度每上升10℃,器件失效率以近2倍的速率上升,实现对IGBT的结温检测对其寿命预测、健康管理有重大意义。但目前现有的各类IGBT结温检测方案中,物理检测法受限于测得温度与结温存在不可避免的误差;光学检测法需要破坏模块封装,无法实现在线监测;热网络法受制于模块老化,需要不断更新参数,工程中难以实践;热敏电参数法是最具潜力的IGBT结温监测方案,而大电流下饱和压降是最常用的热敏电参数之一,其具有侵入性低、外围电路简单、灵敏度高等优点。但由于IGBT存在键合线等连接件阻抗,导致IGBT饱和压降的测量精度受限,从而难以提高结温监测的精度,同时现有IGBT大电流下饱和压降方案中存在的"拐点问题"也限制了结温监测灵敏度的提升,实践工作中提出的IGBT结温检测优化方案正契合目前技术上存在的痛点,也会是毕业论文中重要的一部分内容。

(二)取得的业绩(代表作)【限填3项,须提交证明原件(包括发表的论文、出版的著作、专利证书、获奖证书、科技项目立项文件或合同、企业证明等)供核实,并提供复印件一份】

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Design and Performance Evaluation of a Short-circuit Protection Scheme for SiC MOSFETs	国际期刊	2023年03 月24日	2022 19th China Internatio nal Forum on Solid State Lighting & 2022 8th Internatio nal Forum on Wide Bandgap Semiconduc tors (SSLCHINA: IFWS)		
Dynamic Performance of 6.5kV/400A SiC MOSFET Module and its Gate Driver	国际期刊	2024年05 月09日	2023 IEEE 7th Conference on Energy Internet and Energy System Integratio n (EI2)		
一种基于IGBT饱和压降 拐点的结温检测方法	发明专利申请	2024年09 月27日	申请号: CN 2024108062 31.5		

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课程成绩情况	按课程学分核算的平均成绩: 88 分	
专业实践训练时间及考核情况(具有三年及以上 工作经历的不作要求)	累计时间: 1 年 (要求1年及以上) 考核成绩: 84 分	
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学位证书号:					毕业证书号:			授予学位:		<u></u>		
学习时间	课程名称		备注	学分	成绩	课程性质	学习时间	课程名称	备注	学分	成绩	课程性质
2022-2023学年秋季学期	新能源发电与变流技术			2. 0	95	专业学位课	2022-2023学年春季学期	电气装备健康管理		2. 0	88	专业选修课
2022-2023学年秋季学期	新时代中国特色社会主义理论与	实践		2. 0	94	专业学位课	2022-2023学年春季学期	科技创新案例探讨与实战		2. 0	92	专业选修课
2022-2023学年秋季学期	工程技术创新前沿			1. 5	83	专业学位课	2022-2023学年春季学期	数学建模		2.0	86	专业选修课
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2022-2023学年秋冬学期	高阶工程认知实践			3. 0	83	专业学位课	2022-2023学年夏季学期	研究生英语基础技能		1.0	免修	公共学位课
2022-2023学年冬季学期	综合能源系统集成优化			2. 0	92	专业学位课	2022-2023学年夏季学期	研究生英语		2.0	免修	专业学位课
2022-2023学年秋冬学期	研究生论文写作指导			1.0	92	专业选修课		硕士生读书报告		2.0	通过	
2022-2023学年春季学期	自然辩证法概论			1.0	89	专业学位课						
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说明: 1. 研究生课程按三种方法计分: 百分制,两级制(通过、不通过),五级制(优、良、中、及格、不及格)。

2. 备注中"\*"表示重修课程。

学院成绩校核章 成绩校核人: 张梦依

打印日期: 2025-03-20

#### Design and Performance Evaluation of a Short-circuit Protection Scheme for SiC MOSFETs

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#### **Abstract**

Compared to other silicon-based devices, silicon carbide (SiC) MOSFETs suffer from a shorter short-circuit withstand time and degradation after repeated short-circuiting, which challenges the short-circuit protection circuit design for SiC MOSFETs. In this paper, a short-circuit test platform for SiC MOSFETs is designed and built. Based on the test platform, the relationship between gate voltage, short-circuit withstand time and the short-circuit peak current overshoot is measured and discussed. Based on the test results, a lower gate voltage can significant increase the short circuit withstand time and decrease the short-circuit current. And a short-circuit protection scheme with a soft turn off circuit is proposed and designed, which can achieve fast short-circuit protection response with reduced fault peak current under hard switching fault condition. The soft turn-off circuit can also effectively suppress the voltage overshoot caused by the power loop stray inductance. Compared to the hard turn-off condition, the voltage overshoot can be reduced from 124V to 40V at the same condition using soft-turn off.

#### 1. Introduction

Silicon carbide (SiC) power semiconductors are attracting more and more attention due to their inherent characteristics e.g. higher breakdown voltage, lower power loss, fast switching speed, and higher operating temperature, which bring great benefits in efficiency, weight, size, and control bandwidth in application. And SiC MOSFETs are considered to replace silicon (Si) insulated gate bipolar transistors (IGBTs) in many applications for better performance, such as electric vehicles, space exploration, power systems and other applications. However, current studies show that compared to Si IGBTs, SiC MOSFETs still have weaker short circuit (SC) capabilities than the Si IGBT counterpart, e.g. shorter SC withstand time and risk of degradation after repeated short-circuits[1][2].

Short-circuit protection (SCP) of SiC MOSFETs has been extensively investigated. The desaturation method widely used for IGBT SCP can also be adopted for SiC MOSFET[3-5]. However, compared to Si IGBTs, the boundary between the active and the saturation regions of SiC MOSFETs is not obvious, which makes the threshold and blanking time setting more difficult. A SCP circuit based on Hall sensors is proposed in [6], but the response time is still limited. A shortcircuit protection circuit based on Rogowski coils is proposed in [7], but the noise in signal path can cause malfunction of protection circuit. A SCP method using PCB Rogowski coil is proposed in [8], but the design of the circuit is too complex. A SCP circuit based on gate voltage detection is proposed[9]. However, this method has complex structure, complicated logic and low stability. A voltage source SCP based on field programmable gate array (FPGA) is designed[10]. Due to the large blanking time, the response time of the protection is limited. A reliable and fast response SCP method for SiC MOSFET is still a challenge in the real applications.

In this paper, an SC test platform for SiC MOSFET is designed and built. Its operating principles and implantation are described in detail, and the correlation between gate voltage and SC withstand time/SC current overshoot is investigated. Then, the test platform is used to test the SC withstand capability of SiC MOSFETs at different gate voltages. The experiment results validate that the protection scheme can turn off the short-circuit current in a short time, and effectively suppress the SC peak current and voltage overshoot. Finally, this paper designs a soft turn-off method, which can significantly suppress the voltage overshoot caused by the rapidly dropping fault current and protect the device by preventing gate voltage from surging.

#### 2. Short Circuit Test platform setup

The diagram of the SC test platform is shown in Fig. 1. The capacitor  $C_1$  is used for energy storage. It provides short circuit energy during the test. The capacitor  $C_2$  and capacitor  $C_3$  are used as high frequency decoupling to minimize the stray inductance in the test loop. And they provide high frequency current path during the test to avoid potential parasitic oscillation because the  $C_1$  is usually located a bit far from the device under test (DUT). An IGBT is inserted between the capacitors, which is used as solid-state-circuit-breaker (SSCB) to protect the DUT during the test once the current exceeds a certain level.

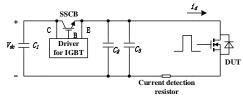


Fig. 1. Short-circuit test platform

During the SC test, a gate pulse is applied to the DUT, and the on-time pulse width of the SC pulse gradually increases until the device is damaged to test its SC withstand time.

The solid-state circuit breaker (SSCB) circuit is shown in Fig. 2, which consists of an IGBT and its overcurrent protection. When the DUT exceeds its preset threshold, the IGBT will be turned off to separate the energy storage capacitor  $C_1$  from the main loop to avoid drastic damage. The protection current is higher than the short circuit current of the DUT.

# Dynamic Performance of 6.5kV/400A SiC MOSFET Module and its Gate Driver

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Abstract—Compared with traditional silicon devices, silicon carbide (SiC) device has outstanding advantages in high frequency, high voltage and high temperature applications. At present, most commercially available SiC devices are low voltage and low power SiC MOSFETs, the dynamic performance of high-voltage and high-current power modules is seldom reported. The dynamic performances of a newly developed SiC MOSFET module under different test environments are studied. The related gate drive for this high voltage SiC module is also discussed. From the aspects of driving resistance  $R_{\rm g}$ , operating junction temperature  $T_{\rm j}$ , load current Id, bus voltage  $V_{\rm ds}$ , the dynamic and short-circuit characteristics of a 6.5kV/400A SiC MOSFET are fully evaluated. The experimental results will help to optimize the device design and engineering application for high-voltage, high-current SiC devices.

Keywords—SiC MOSFET, dynamic characteristics, short-circuit characteristics

#### I. INTRODUCTION

With the development of wide bandgap device, SiC MOSFETs are more and more widely used in power converters. Compared with silicon-based devices, SiC materials have higher band gap, breakdown field strength and thermal conductivity. SiC devices show obvious advantages in terms of on-state loss. switching speed, and operating temperature, which can meet more extensive application requirements[1]. At present, most commercial SiC modules have voltage levels of 1.2kV and 1.7kV. Although CREE released a 6.5kV/340A SiC MOSFET module[2], there are still few high-voltage and high-current silicon carbide devices reported. Besides the technical challenges, another major constraint is performance testing and reliability issues. Although SiC devices have higher thermal conductivity to improve their thermal characteristics, due to their smaller chip area and higher current density, SiC devices have a shorter short-circuit withstand time than silicon-based devices[3]. Furthermore, as the switching speed of SiC devices increases, although high di/dt and dv/dt in the switching transient help reduce the switching loss of the device, it will cause severe EMI problems, and bring new insulation challenges to real applications. Therefore, it is particularly important to study the transient characteristics of SiC MOSFETs.

Since nearly 2/3 of the failure faults of power electronic devices are caused by thermal stresses, and most of them are caused by overheating damage due to the transient energy accumulated from short-circuit faults, it is necessary to study the short-circuit characteristics of SiC MOSFETs at high temperatures.

This paper will provide a detailed dynamic performance evaluation for a new developed  $6.5 \mathrm{kV/400A}$  SiC MOSFET module. A digital gate driver with short-circuit protection, active clamping is designed, and the dynamic test platform for SiC MOSFET with low parasitic parameters is also developed. Based on the principles of controlled variables, the switching transient evaluation was carried out with different drive resistance  $R_g$ , operating junction temperature  $T_j$ , load current Id, bus voltage  $V_{ds}$ , etc. And the short-circuit characteristics of the SiC MOSFET under high temperature are studied too. According to the experimental results, the dynamic characteristics of the SiC MOSFET is evaluated and analyzed.

## II. DESIGN OF DYNAMIC TEST PLATFORM AND GATE DRIVER CIRCUIT

In order to evaluate the effect of various parameters on the switching transient characteristics of SiC MOSFET accurately and reliably, and reduce the measurement error caused by

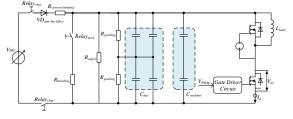


Fig. 1. Schematic diagram of double pulse test circuit

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## (12) 发明专利申请



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#### (54) 发明名称

一种基于IGBT饱和压降拐点的结温检测方法

#### (57) 摘要

本发明属于电力电子技术领域,公开一种基于IGBT饱和压降拐点的结温检测方法,包括以下步骤:根据不同结温下的饱和压降和集电极电流信息,获得IGBT饱和压降拐点电压和拐点电流信息;根据拐点电压和拐点电流信息,获得等效压降;建立数据库,该数据库包括等效压降、集电极电流、结温的对应关系;根据测得的饱和压降、集电极电流、以及所述拐点电压和拐点电流信息,获得等效压降,再根据等效压降、集电极电流信息在所述数据库中获得对应的结温数据。本发明的方法可以消除IGBT饱和压降测量值中连接件阻抗所造成的误差,有效提高IGBT在线结温检测器的精度。



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