同行专家业内评价意见书编号：20250855094

附件1

浙江工程师学院（浙江大学工程师学院）
同行专家业内评价意见书

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申报工程师职称专业类别（领域）：机械

浙江工程师学院（浙江大学工程师学院）制

2025年03月11日

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一、个人申报

（一）基本情况【围绕《浙江工程师学院（浙江大学工程师学院）工程类专业学位研究生工程师职称评审参考指标》，结合该专业类别(领域)工程师职称评审相关标准，举例说明】

1.对本专业基础理论知识和专业技术知识掌握情况(不少于200字)

本人系统掌握了机械工程专业基础理论与技术知识体系。在基础理论层面，通过核心课程学习，建立了机械结构分析、有限元建模等理论基础，能运用MATLAB完成理论分析建模，运用COMSOL开展多物理场仿真。行业技术知识方面，系统学习几何公差标准，在实习中标准制造流程，参与实际零部件设计。工程实践层面，在教育部A类赛事铸造大赛中主导铸造方案设计，完成浇注系统设计、铸造工艺参数计算、工艺方案优化、砂芯及工装设计。跨学科领域，选修《电子与通信工程领域前沿讲座》课程，持续关注先进半导体领域技术动态。

2.工程实践的经历(不少于200字)

本人深度参与了企业科研项目的工程实践：12英寸硅片最终抛光设备的研制及应用，在项目中承担任务包括有针对新设备高转速抛光盘的需求，对原设计抛光盘组件的各种零件进行分析并简化，提出一种特殊螺栓互锁调平机构，设计内封焊接水道，降低抛光盘自身负载，实现转速提升；针对客户对撕贴垫的要求以及隔绝金属污染的风险，制定特氟龙性能指标，对不同抛光盘面特氟龙材质性能进行探索，优化工艺设计，最终获得良好的硬度、粗糙度、膜厚差；根据整机布置情况以及各组件要求，确定整机水气路设计要求，完成零部件选型以及水气路的设计搭建。最终成功完成预期目标，实现先进硅片抛光设备的研制。

3.在实际工作中综合运用所学知识解决复杂工程问题的案例（不少于1000字）

最终抛光是利用化学机械协同效应，通过抛光液、磨粒和抛光垫的相互作用在硅片表面实现纳米级材料去除的技术。该技术可获得高洁净度和高平整度的硅片表面，满足后续芯片制造需求。最终抛光的工艺参数易于调整，且硅片间的一致性较好，是应用于硅片制造的最后一道工序，对硅片表面质量具有决定性作用。然而，在工业界实际应用时，面临以下挑战：1)大尺寸硅片表面的材料去除均匀性控制难：与8英寸硅片相比，12英寸硅片的面积显著增加，厚度却仅提升约6.9%，这使得硅片在最终抛光过程中更容易出现去除不均匀等问题，增加了最终抛光工艺调试的难度；2)表面纳米形貌质量低：随着芯片制程的不断提高，短空间波长下表面纳米形貌质量将直接影响后续芯片制造光刻性能、薄膜均匀性、器件良率以及键合质量，目前硅片制造中仅依赖单一的双面抛光工序无法获得高质量表面纳米形貌；3)当前抛光组件以生产小尺寸硅片为主：我国抛光设备当前生产的主流硅片仍以8英寸为主，12英寸硅抛光片质量相较国际尖端产品仍存在差距，无法满足日益增长的12英寸硅片市场需求。针对上述工程问题，本人在企业实践过程中，综合运用所学知识解决复杂工程问题的案例如下：

(1)大尺寸硅片最终抛光设备结构设计方面，在企业实践过程中调研了大尺寸硅片最终抛光的原理，了解集成电路工业生产实践需求，分析大尺寸硅片的抛光工艺要求，深度参与企业的最终抛光设备的关键零部件结构设计，实现大尺寸硅片的加工精度达到ΔGBIR＜30%、ΔSFQR＜30%、ΔESFQR＜40%。

(2)大尺寸硅片最终抛光去除模型方面，目前研究关于最终抛光去除率分布情况的研究较为欠缺，仅能得出总去除率大小，这导致无法有效预测晶圆的表面形貌，使去除模型在实际的工业应用中受到限制。针对此问题，考虑了化学反应过程造成的材料去除，建立起一个可精确计算去除率以及去除率分布情况的模型。

(3)大尺寸硅片最终抛光建模与仿真分析方面，目前的数值模拟研究大都为仅针对硅片表面建模的二维仿真模型，缺少对整个抛光结构的仿真研究，这导致与实际抛光过程不相符，很

难反映真实的流动与传质传热情况。针对目前学术界和工业界对抛光过程了解匮乏的现状，建立了一个完整考虑大尺寸硅片单面化学机械最终抛光过程的多物理场耦合模型，为最终抛光的应用提供理论基础。

(4)硅片最终抛光热场测试与抛片实验方面，在抛光过程由于存在化学反应和磨粒摩擦作用不断产热，硅片表面温度升高，从而影响抛光质量。通过调整优化工艺参数，获得不同工艺参数对其影响规律，最终得出较优的工艺参数组合进行大尺寸硅片的最终抛光实验，实现了稳定均匀的材料去除，获得了优良的表面几何形貌和纳米形貌，已成功应用于大尺寸硅片制造。

(5)硅片表面纳米形貌表征与调控方面，抛光垫作为磨粒的载体，其与硅片间的接触状态将对抛光后的表面纳米形貌产生直接影响。针对先进制程对硅片表面纳米形貌质量的要求不断提高的工程需求，在企业实践中对硅片表面纳米形貌进行测试与表征，深入分析抛光垫的纹理、硬度和结构特性对最终抛光过程对表面纳米形貌的影响规律，最终获得了满足集成电路制造要求的高质量硅抛光片。

（二）取得的业绩（代表作）【限填3项，须提交证明原件（包括发表的论文、出版的著作、专利证书、获奖证书、科技项目立项文件或合同、企业证明等）供核实，并提供复印件一份】					
1. 公开成果代表作【论文发表、专利成果、软件著作权、标准规范与行业工法制定、著作编写、科技成果获奖、学位论文等】					
成果名称	成果类别 [含论文、授权专利（含发明专利申请）、软件著作权、标准、工法、著作、获奖、学位论文等]	发表时间/授权或申请时间等	刊物名称/专利授权或申请号等	本人排名/总人数	备注
Numerical modeling and experimental study of thermal field and material removal for silicon wafer in final-touch polishing	TOP期刊	2025年01月05日	Journal of Manufacturing Processes	1/4	
Measurement of Thermal Field Temperature Distribution Inside Reaction Chamber for Epitaxial Growth of Silicon Carbide Layer	权威期刊	2024年04月22日	ASME Journal of Manufacturing Science and Engineering	1/5	
硅外延生长反应腔内外延反应过程的数值仿真建模及实验研究	核心期刊	2024年03月01日	机械工程学报	1/6	

2.其他代表作【主持或参与的课题研究项目、科技成果应用转化推广、企业技术难题解决方案、自主研发设计的产品或样机、技术报告、设计图纸、软课题研究报告、可行性研究报告、规划设计方案、施工或调试报告、工程实验、技术培训教材、推动行业发展中发挥的作用及取得的经济社会效益等】

（三）在校期间课程、专业实践训练及学位论文相关情况	
课程成绩情况	按课程学分核算的平均成绩： 86 分
专业实践训练时间及考核情况(具有三年及以上工作经历的不作要求)	累计时间： 1.2 年（要求1年及以上） 考核成绩： 87 分
本人承诺	
个人声明：本人上述所填资料均为真实有效，如有虚假，愿承担一切责任，特此声明！ **申报人签名：**邓世伟	

2226024

二、日常表现考核评价及申报材料审核公示结果

日常表现考核评价	非定向生由德育导师考核评价、定向生由所在工作单位考核评价： ☑优秀 ☐良好 ☐合格 ☐不合格 德育导师/定向生所在工作单位分管领导签字（公章）：　　年　月　日
申报材料审核公示	根据评审条件，工程师学院已对申报人员进行材料审核（学位课程成绩、专业实践训练时间及考核、学位论文、代表作等情况），并将符合要求的申报材料在学院网站公示不少于5个工作日，具体公示结果如下： ☐通过 ☐不通过（具体原因：　　） 工程师学院教学管理办公室审核签字（公章）：　　年　月　日

浙 江 大 学 研 究 生 院

攻读硕士学位研究生成绩表

学号：22260024	姓名：邓世伟	性别：男	学院：工程师学院	专业：机械	学制：2.5年
毕业时最低应获：26.0学分		已获得：28.0学分		入学年月：2022-09	毕业年月：
学位证书号：			毕业证书号：		授予学位：

学习时间	课程名称	备注	学分	成绩	课程性质	学习时间	课程名称	备注	学分	成绩	课程性质
2022-2023学年秋季学期	工程技术创新前沿		1.5	85	专业学位课	2022-2023学年秋冬学期	研究生论文写作指导		1.0	88	专业选修课
2022-2023学年秋季学期	“四史”专题		1.0	94	公共选修课	2022-2023学年秋冬学期	研究生英语		2.0	86	专业学位课
2022-2023学年秋季学期	研究生英语基础技能		1.0	65	公共学位课	2022-2023学年春季学期	电子与通信工程领域前沿讲座		2.0	94	专业选修课
2022-2023学年秋冬学期	智能工业机器人及其应用		3.0	87	专业选修课	2022-2023学年春季学期	自然辩证法概论		1.0	83	专业学位课
2022-2023学年秋冬学期	工程伦理		2.0	73	专业学位课	2022-2023学年春夏学期	人工智能制造技术		3.0	92	专业学位课
2022-2023学年冬季学期	产业技术发展前沿		1.5	86	专业学位课	2022-2023学年春夏学期	高阶工程认知实践		3.0	83	专业学位课
2022-2023学年冬季学期	工程中的有限元方法		2.0	100	专业选修课		硕士生读书报告		2.0	通过	
2022-2023学年冬季学期	新时代中国特色社会主义理论与实践		2.0	92	专业学位课						

说明：1.研究生课程按三种方法计分：百分制，两级制（通过、不通过），五级制（优、良、中、及格、不及格）。

2.备注中“*”表示重修课程。

学院成绩校核章：

成绩校核人：张梦依

打印日期：2025-03-20

浙江大学研究生 (60) 成绩校核章

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Numerical modeling and experimental study of thermal field and material removal for silicon wafer in final-touch polishing

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ARTICLE INFO

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Final-touch polishing
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ABSTRACT

With the rapid development of semiconductor industry, large-sized silicon wafers with high flatness and uniform nanotopography are generally required. Final-touch polishing (FP) is the final process in silicon wafer production, it can effectively clean the wafer's surface and control its surface geometry. The distribution of thermal field during final-touch polishing process is challenging to measure and predict, it greatly affects the characteristics and non-uniformity of material removal profile in both mechanical and chemical aspects. This study develops a numerical model to study the thermal field distribution and material removal, and used to predict the thermal characteristics and material removal profile of silicon wafer during final-touch polishing. For validation, an infrared camera and infrared sensor were applied to measure the surface temperature during polishing, and the surface material removal profile was examined and compared with model predictions. The surface material removal profile was also performed to investigate the effects of polishing parameters, including slurry flow rate, rotational speed and applied pressure. By obtaining optimal polishing parameters, final-touch polishing experiments were conducted on 12-inch silicon wafers. The experimental results showed that the polished silicon wafer has a highly flat surface with flatness of site front least square range was 23.06 nm and edge site front least square range was 23.77 nm, and the nanotopography threshold values of 2×2 mm^2 area and 10×10 mm^2 area (THA2 & THA10) for polished silicon wafer were 7.21 nm and 17.72 nm can be achieved, respectively.

1. Introduction

Large-sized silicon wafers (8 in. and above) have been widely used in semiconductors to fabricate integrated circuit chips [1]. With the continuous development of ultra-large scale integrated circuits (ULSI), the silicon wafer's surface quality requirement should have low defects, high flatness and uniform nanotopography [2]. Deterioration in surface geometry of large-sized silicon wafers not only influences the surface flatness but also raises challenges for subsequent lithographic focus [3,4]. Final-touch polishing (FP) is the final process of fabricating high quality silicon wafers with high flatness, stable, and uniform material removal [4]. During final-touch polishing, the material removal characteristics exhibit highly sensitive to fabrication conditions, such as applied contact pressure [5], abrasive contact status [6], temperature distribution [7] and chemical reaction intensity [8,9], thus would lead to deterioration in material removal uniformity.

The fabrication of 12-inch silicon wafers mainly includes three key polishing processes: double-sided polishing (DSP), edge polishing (EP), and final-touch polishing. All three processes utilize the mechanism of chemical mechanical polishing (CMP) to remove wafer surface material effectively. The DSP mainly achieves stock removal on the wafer surface (about 15 μm) and obtains the surface flatness and nanotopography [10]. In the EP process, the material removal of the wafer's bevel occurs to obtain the clean edge, reduce residual stress and prevent fragmentation [11]. In the FP process, it requires to minimize deterioration for high flatness and nanotopography obtained after DSP process, it also aimed to achieve particle free with mirror surface finishing [12]. In a typical final-touch polishing process, a fast polishing procedure is followed by two fine polishing procedures. The fast polishing achieves major material removal (about 300 nm–600 nm) to reach the desired surface geometry, while fine polishing primarily focuses on surface cleaning and reducing residual metals. The physical and chemical

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Measurement of Thermal Field Temperature Distribution Inside Reaction Chamber for Epitaxial Growth of Silicon Carbide Layer

Silicon carbide (SiC) has been widely utilized in the semiconductor industry for the development of high-power electrical devices. Using chemical vapor deposition to grow a thin epitaxial layer onto the SiC substrate surface with orderly lattice arrangement, good surface morphology, and low doping concentration is required. During epitaxial growth, the high reaction temperature and its distribution are generally difficult to measure and will affect the properties of the epitaxial growth layer. This study presents a thermal-field testing method based on process temperature control rings (PTCRs) to measure the high-temperature distribution inside the epitaxial growth reaction chamber, and to study the effects of reaction chamber structure and epitaxial growth parameters on the quality of the epitaxial layer. The measurement accuracy of PTCRs was characterized using silicon melting experiments and the measuring principle of PTCRs was presented. The thermal field of the reaction chamber was then numerically simulated and compared with experimental results. The experiment results exhibit a temperature gradient of less than 0.4 °C/mm on the surface, indicating good temperature uniformity. Epitaxial growth is an essential process in the fabrication of SiC devices, as it enables the production of layers with precise doping density and thickness. The SiC epitaxial growth experiments were conducted to study the effects of the gas flow ratio and doping flow ratio of three inlet flow channels on the thickness and doping concentration distributions. The results demonstrated that the non-uniformity of thickness and doping concentration of the epitaxial layer were below 1.5% and 4.0%, respectively. [DOI: 10.1115/1.4065021]

Keywords: silicon carbide, epitaxial growth, temperature characterization, reaction chamber, gas flowrate, micro- and nano-machining and processing, nontraditional manufacturing processes

1 Introduction

Silicon carbide (SiC) is a well-known semiconductor material that has been widely used for high-power and high-frequency electronic devices such as power electronics, automotive electronics, and communication devices [1–4]. Due to the high covalent nature of the Si–C bond, efficient lattice vibration conduction increases the group velocity of phonons, thus enhancing the thermal conductivity (~5 W/cm·K) [5,6]. Additionally, SiC exhibits a wide bandgap, with high electron saturation velocity (~2×10^7 cm/s) and critical electric field strength (~3 MV/cm) [7]. The relatively high crystal dislocation density in commercial SiC substrate (10^3–10^4 cm^{-2}) will greatly affect its performance [8–10]. Therefore, to fabricate high-performance power devices, it is crucial to grow a low roughness epitaxial SiC layer on the substrate surface with uniform thickness and doping concentration, as well as a complete and ordered crystal lattice without defects including carrot defect [11], triangular defect [12], downfall [13], and step bunching [14].

Several methods have been proposed for the growth of SiC epitaxial layers onto the substrate surface, such as physical vapor transport [15], liquid phase epitaxy [16], molecular beam epitaxy [17], pulsed laser deposition [18], and chemical vapor deposition (CVD). The CVD is able to achieve a high-quality homo-epitaxial growth of SiC epitaxial layer through step-flow growth, which leads to fewer defects and moderate growth rates [19,20]. As shown in Fig. 1, the reaction source gases of $SiHCl_3$ (TCS) and C_2H_4 are introduced into an epitaxial growth reaction chamber under the carrier gas of H_2, where intermediate compounds are generated through gas phase reaction. These compounds are adsorbed on the substrate surface through gas phase diffusion into the boundary layer, and further generate carbon atoms, silicon atoms, and byproducts via surface reaction. Some of the carbon and silicon atoms diffuse through the surface to the correct position and incorporate into the lattice to form the epitaxial layer, while the rest are desorbed from the surface together with byproducts and discharged with the main gas flow. Thus, the CVD epitaxial growth of SiC is a complex reaction process that requires precise control of gas flowrate,

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硅外延生长反应腔内外延反应过程的数值仿真建模及实验研究*

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摘要：硅外延片是大规模集成电路、半导体器件等的基础功能材料，是通过外延反应在单晶硅片上生长均匀的外延薄层。外延层的厚度和电阻率的均匀性控制是硅外延生长的关键技术难题，其生长质量受反应腔室的结构与热流场设计影响较大。基于单片式硅外延生长反应腔室的结构，建立了反应腔内气体输运与外延反应的多物理场仿真模型，分析了腔室结构对热场分布均匀性的影响规律。随后通过数值仿真，研究了载气流量、进气梯度、基座转速等工艺参数对硅外延生长反应过程的影响。随后，开展了反应腔内多测点温度的测试实验，结果表明不同工艺条件下数值仿真预测的温度与实测的温度分布及变化规律相较一致，最大温度预测偏差< 1.2%。基于仿真分析，获得了优化的外延生长工艺参数组合，并开展了 200 mm 硅外延生长反应实验，测试结果表明硅外延层的厚度不均匀性< 0.76%，电阻率不均匀性< 1.58%，满足集成电路硅片制造所需的外延层高品质生长要求。

关键词：硅外延层；外延生长；化学气相沉积；热流场；反应腔室

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Numerical Modeling and Experimental Study of the Reaction Process in Silicon Epitaxial Growth Reaction Chamber

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Abstract: Silicon epitaxial wafer is the basic functional material for large scale integrated circuits and semiconductor devices, etc. It is the growth of uniform epitaxial thin layer on single crystal silicon wafer through epitaxial reaction, the uniformity control of epitaxial layer's thickness and electrical resistivity is the key challenge of silicon epitaxial growth. The growth quality of silicon epitaxial layers is significantly influenced by the design of reaction chamber and thermal flow field. A multi-physics field simulation model to analyze the effects of chamber structure on the uniformity of thermal field distribution is established. Additionally, the effects of process parameters such as carrier gas flow rate, inlet gradient and susceptor speed on the silicon epitaxial growth reaction process through numerical simulation are investigated. Experimental results from multi-point temperature tests of reaction chamber demonstrate a high level of agreement between predicted and measured temperature distributions under different process conditions, with a maximum temperature prediction deviation < 1.2%. Based on the simulation analysis, an optimized combination of epitaxial

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