同行专家业内评价意见书编号：20240854189

附件1

浙江工程师学院（浙江大学工程师学院）
同行专家业内评价意见书

姓名：冯威威

学号：22160568

申报工程师职称专业类别（领域）：电子信息

浙江工程师学院（浙江大学工程师学院）制

2024年03月21日

一、个人申报

（一）基本情况【围绕《浙江工程师学院（浙江大学工程师学院）工程类专业学位研究生工程师职称评审参考指标》，结合该专业类别(领域)工程师职称评审相关标准，举例说明】

通过参与“基于ZYNQ的雷达信号分析系统研究”项目，使我的专业基础理论知识和专业技术得到了深化和提升，我深刻地体会到项目实践对知识掌握、能力提升和素质养成的重要意义，结合我的个人成长和企业实践，我将分享以下情况：

1. 知识掌握与能力提升：

在项目中，我深入学习了ZYNQ硬件平台和FPGA技术，学会了使用Verilog进行硬件描述和设计。通过与团队成员的合作，我掌握了高速信号处理、干扰信号生成和系统控制等关键技术。在实践中，我不断钻研优化算法和硬件设计，提高了系统的性能和效率。通过这个项目，我不仅学到了专业知识，还培养了分析和解决问题的能力，对于复杂项目的开发和实施有了更深刻的理解。

2. 项目管理与协作能力：

在项目中，我负责与团队成员协作，确保项目按时交付。我积极主动地参与讨论和决策，提供技术支持和解决方案。通过与团队的密切合作，我学会了项目管理和沟通技巧，提高了自己的协作能力和团队合作精神。在项目中，我还学会了分配任务和监督进度，使团队工作高效有序。这些经验将对我的职业生涯和未来的项目实践有很大的帮助。

3. 创新思维与问题解决能力：

在项目中，我面临着各种技术难题和挑战。通过不断的尝试和探索，我积极寻找新的解决方案，培养了创新思维和问题解决能力。在解决问题的过程中，我学会了从不同角度分析和思考，提高了自己的逻辑思维和决策能力。这些经验使我成为一个更加灵活和适应性强的工程师。

4. 专业精神与责任心：

在项目中，我时刻保持着对技术的热情和专注。我不断追求技术的完美和创新，对每一个细节都严格把控，确保项目的质量和成果。在面对项目的挑战和压力时，我从不退缩，始终保持着积极的态度和坚定的信念。我深刻理解技术对于企业发展的重要性，对于工程师的责任和使命有了更深刻的认识。

5. 个人成长与企业实践结合：

通过“基于ZYNQ的雷达信号分析系统研究”项目，我深刻体会到学习与实践的结合是个人成长的关键。在项目中，我将所学的理论知识与实际应用相结合，不断地总结经验和教训。我学会了如何在项目中不断挑战自己、突破自己，不断提高自己的技术和能力。同时，我也深刻理解企业实践对于个人发展。

工程实践经历：

通过“基于ZYNQ的雷达信号分析系统研究”项目，我们成功研制了一款适用于多种场景的雷达信号分析系统，该系统能够截获雷达信号，并对雷达信号的信号参数进行准确分析。之后根据分析结果，我们能够生成相应的干扰信号，包括欺骗干扰、压制干扰、宽带干扰等多种干扰形式。这一项目成果解决了信号探测和分析的重要问题。

取得的经济和社会效益：

通过“基于ZYNQ的雷达信号分析系统研究”项目的研制和应用，我们为雷达信号分析领域作出了重要贡献。该系统的成功研制，增强了对雷达信号的截获和分析能力。同时，该项目的成果还为我国电子对抗技术的发展做出了重要贡献，推动了我国电子对抗领域的技术创新和产业发展。

工程问题案例：

在“基于ZYNQ的雷达信号分析系统研究”项目中，存在以下主要难点：
高速信号处理：在本项目中，高速信号处理是一个核心难题。雷达信号的连续高速采集对FPGA的处理能力提出了极高的要求。系统需要能够在极短的时间内完成对信号的采集、处理和分析，确保对敌方雷达信号的实时性和准确性分析。这不仅涉及到硬件平台的选择，还包括对信号处理算法的优化，以实现快速有效的数据处理。
干扰信号生成：干扰信号的生成是另一个技术难点。系统需要根据实时分析的雷达信号参数动态调整，以生成复杂多样的干扰信号。这要求FPGA不仅要具备高效的信号处理能力，还需要能够在短时间内根据分析结果生成相应的干扰信号，包括欺骗干扰、压制干扰和宽带干扰等。
系统控制与优化：系统的控制与优化也是项目成功的关键。ARM处理器在本系统中承担着对整个系统进行控制和监控的任务。它不仅需要实现对干扰信号的精确控制，还要负责对敌方雷达信号进行实时分析，以优化干扰效果。这就要求处理器具备高效的算法和优化策略，以保证系统的实时性和高效性。
针对以上难点，运用所学知识设计了以下技术路线：
该雷达信号分析系统采用ZYNQ硬件平台，结合FPGA和ARM处理器，充分发挥两者的优势。其中，FPGA负责高速信号处理和实时干扰信号生成，ARM处理器负责系统的控制、信号参数分析和用户界面。具体技术流线如下：
信号采集：使用ZYNQ硬件平台中的ADC模块对敌方雷达信号进行高速连续采集，确保实时性和准确性。
信号处理：利用FPGA进行快速信号处理，包括滤波、FFT变换和信号参数提取，以获取敌方雷达信号的频率、幅度和相位信息。
干扰信号生成：根据分析得到的敌方雷达信号参数，利用FPGA实时生成干扰信号，包括欺骗干扰、压制干扰和宽带干扰，以对敌方雷达系统产生影响。
控制与分析：通过ARM处理器对整个系统进行控制和监控，实现对干扰信号的精确控制。同时，ARM处理器负责对敌方雷达信号进行实时分析，以优化干扰效果。
同时为了进一步提升系统性能，综合运用所学知识，还对后续的实践工作的优化路线做出如下安排：
优化算法：针对高速信号处理和干扰信号生成，优化FPGA中的算法和数据处理流程，提高系统的处理速度和效率。
硬件优化：考虑采用更高性能的ADC和DAC芯片，提高信号采集和输出的精度和速度。
干扰策略优化：对于不同类型的雷达信号，研究并优化不同的干扰策略，以提高干扰效果和隐蔽性。
系统稳定性：考虑添加自适应控制算法，使系统能够在不同环境下自动调整参数，保持稳定的干扰效果。
通过上述技术路线和优化策略的实施，"基于ZYNQ的雷达信号分析系统"项目旨在开发出一套能够有效应对现代电子战挑战的高性能雷达信号分析与干扰系统。该系统的研发不仅能够提升我方在电子对抗领域的技术水平，还将为未来相关技术的发展奠定坚实的基础。

（二）取得的业绩（代表作）【限填3项，须提交证明原件（包括发表的论文、出版的著作、专利证书、获奖证书、科技项目立项文件或合同、企业证明等）供核实，并提供复印件一份】					
1. 公开成果代表作【论文发表、专利成果、软件著作权、标准规范与行业工法制定、著作编写、科技成果获奖、学位论文等】					
成果名称	成果类别 [含论文、授权专利（含发明专利申请）、软件著作权、标准、工法、著作、获奖、学位论文等]	发表时间/授权或申请时间等	刊物名称/专利授权或申请号等	本人排名/总人数	备注
Research on High-Speed Detection Method of Radar Signal Based on RFSoC	会议论文	2024年02月04日	2023 IEEE the 15th International Conference on Wireless Communications and Signal Processing	1/4	

2.其他代表作【主持或参与的课题研究项目、科技成果应用转化推广、企业技术难题解决方案、自主研发设计的产品或样机、技术报告、设计图纸、软课题研究报告、可行性研究报告、规划设计方案、施工或调试报告、工程实验、技术培训教材、推动行业发展中发挥的作用及取得的经济社会效益等】

（三）在校期间课程、专业实践训练及学位论文相关情况	
课程成绩情况	按课程学分核算的平均成绩： 85 分
专业实践训练时间及考核情况(具有三年及以上工作经历的不作要求)	累计时间： 1.3 **年**（要求1年及以上） 考核成绩： 89 分（要求80分及以上）
本人承诺	
个人声明：本人上述所填资料均为真实有效，如有虚假，愿承担一切责任，特此声明！ **申报人签名：**	

22160568

二、日常表现考核评价及申报材料审核公示结果

日常表现考核评价	非定向生由德育导师考核评价、定向生由所在工作单位考核评价。 ☑优秀 ☐良好 ☐合格 ☐不合格 德育导师/定向生所在工作单位分管领导签字（公章）：　　年　月　日 2024.3.22.
申报材料审核公示	根据评审条件，工程师学院已对申报人员进行材料审核（学位课程成绩、专业实践训练时间及考核、学位论文、代表作等情况），并将符合要求的申报材料在学院网站公示不少于5个工作日，具体公示结果如下： ☐通过 ☐不通过（具体原因：　　） 工程师学院教学管理办**公室**审核签字（公章）：　　年　月　日

浙 江 大 学 研 究 生 院

攻读硕士学位研究生成绩表

学号：22160568	姓名：冯威威	性别：男	学院：信息与电子工程学院	专业：电子信息	学制：2.5年
毕业时最低应获：24.0学分		已获得：24.0学分		入学年月：2021-09	毕业年月：2024-03
学位证书号：1033532024312012			毕业证书号：103351202402310068		授予学位：电子信息硕士

学习时间	课程名称	备注	学分	成绩	课程性质	学习时间	课程名称	备注	学分	成绩	课程性质
2021-2022学年秋季学期	电子信息工程中数学模型与方法		2.0	86	专业学位课	2021-2022学年秋冬季学期	中国特色社会主义理论与实践研究		2.0	94	公共学位课
2021-2022学年秋季学期	数值计算方法		2.0	92	专业选修课	2021-2022学年春季学期	电子与通信工程领域前沿讲座		2.0	94	专业选修课
2021-2022学年秋季学期	人工智能算法与系统		2.0	85	专业学位课	2021-2022学年春季学期	科学研究与写作指导		1.0	91	专业学位课
2021-2022学年秋冬季学期	大数据基础与应用		2.0	94	专业选修课	2021-2022学年夏季学期	研究生英语		2.0	71	公共学位课
2021-2022学年秋冬季学期	机器学习		3.0	93	专业学位课	2021-2022学年夏季学期	研究生英语基础技能		1.0	66	公共学位课
2021-2022学年秋冬季学期	工程前沿技术讲座		2.0	83	专业学位课	2021-2022学年夏季学期	自然辩证法概论		1.0	91	公共学位课
2021-2022学年冬季学期	工程伦理		2.0	87	公共学位课						

说明：1.研究生课程按三种方法计分：百分制，两级制（通过、不通过），五级制（优、良、中、及格、不及格）。

2.备注中“*”表示重修课程。

学院成绩校核章：

成绩校核人：张梦依

打印日期：2024-04-02

Acceptance Notification Letter

Dear Weiwei Feng, Xiating Wang, Zhiguo Shi, Yong Wang,

Congratulations!

On behalf of the Organizing Committee, we are pleased to inform you that your paper "**Research on High-Speed Detection Method of Radar Signal Based on RFSoC**"（Paper ID:**1570939751**） has been accepted and you are cordially invited to give a presentation at the 15th International Conference on Wireless Communications and Signal Processing (WCSP 2023), which will be held in Hangzhou, China during November 2-4, 2023.

WCSP is an annual International Conference on Wireless Communications and Signal Processing (WCSP). The aim of the conference is to provide an international forum that brings together researchers from academia and practitioners from industry to exchange advances in recent research work on all aspects of wireless communications and signal processing. With the support of all participants, the past fourteen events of the conference have been very successful. We are now organizing WCSP 2023, the fifteenth edition of the conference. You are cordially welcome to participate in and contribute to the conference in your valuable role.

The accepted papers after full registration and in-person presentation will be included into WCSP Conference Proceedings and submitted for inclusion into IEEE Xplore subject to meeting IEEE Xplore's scope and quality requirements, which will be submitted for indexing by Ei Compendex and Scopus.

Once again, congratulations! We look forward to seeing you and having your participation in the conference.

If you need any assistance, please do not hesitate to contact us <wcsp2023@hotmail.com>.

Yours sincerely,

Best Regards,
Conference Committee
WCSP 2023

PUBLICATION GUIDANCE

To register the conference and have your paper included in the conference proceedings successfully, please finish following Five steps.

1. Revise your paper according to reviews carefully.
2. Format your paper according to template carefully.

Latex Template:
https://www.ieee.org/content/dam/ieee-org/ieee/web/org/pubs/conference-latex-template_10-17-19.zip

Word Template:
https://www.ieee.org/content/dam/ieee-org/ieee/web/org/conferences/conference-template-letter.docx

3. Click the registration link and finish the payment before **23:59 September 25, 2023** (Beijing Time): https://iconf.young.ac.cn/BhL4k. More information about registration can be find at http://www.ic-wcsp.org/2023/show.asp?id=22

4.Upload your final papers (PDF or Doc.) to https://iconf.young.ac.cn/iZoLF before **23:59 September 25, 2023** (Beijing Time). Please be kindly informed that Doc. is better for us to revise your paper format.

5. An IEEE e-copyright confirmation will be sent to you after you submit your final paper, please kindly wait for our notification email and always keep an eye to the mailbox even though the conference ends.

Should you require further assistance, please feel free to contact us via wcsp2023@hotmail.com.

For the most updated information on the conference, please check the conference website at http://www.ic-wcsp.org/2023/index.asp.

2023 IEEE the 15th International Conference on Wireless Communications and Signal Processing

Research on High-speed Detection Method of Radar Signal Based on RFSoC

Weiwei Feng[1], Xiating Wang[1], Zhiguo Shi[1,2], Yong Wang[1,2]
[1] College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China
[2] Key Laboratory of Collaborative Sensing and Autonomous Unmanned Systems of Zhejiang Province
E-mail: fengvv@zju.edu.cn, wangxtt@zju.edu.cn, shizg@zju.edu.cn, wangy@zju.edu.cn

2023 International Conference on Wireless Communications and Signal Processing (WCSP) | 979-8-3503-2466-2/23/$31.00 ©2023 IEEE | DOI: 10.1109/WCSP58612.2023.10405269

***Abstract*—This paper proposes a real-time radar signal detection method based on RFSoC and parallel Fast Fourier Transform (FFT) architecture, suitable for electronic warfare (EW) applications in electronic reconnaissance aircraft. The proposed method utilizes high-speed Analog-to-Digital Converters (ADC) and high-performance heterogeneous processing units integrated in RFSoC, combined with parallel FFT algorithm, to optimize the radar signal detection architecture. It improves the time-accuracy trade-off in large point FFT processing, enabling the electronic reconnaissance aircraft to detect radar signals containing any number of carriers with instantaneous bandwidth of 2 GHz and frequency resolution of 1 MHz in 3 us. Both Matlab simulation and real-world experimental results are presented to validate the rationality and reliability of the design, providing a reference for the design of modern high-performance electronic reconnaissance aircraft.**

Keywords—RFSoC, parallel FFT, high-speed detection, radar, instantaneous bandwidth 2GHz

I. Introduction

With the advancement of electronic science and technology, modern warfare has gradually evolved into a new form of information and electronic warfare. Modern combat weapons are not only simple killing tools but also play a significant role in acquiring enemy information. Electronic reconnaissance aircraft have the crucial capability to intercept radar signals in real-time and analyze various parameters, providing essential support for localization [1], interference, deception, and other strike tactics, making them a crucial representative of modern combat weaponry [2].

In modern electronic reconnaissance aircraft, the structure of high-speed ADC combined with FPGA to perform the Fast Fourier Transform on digital signals has effectively improved the shortcomings of traditional electronic reconnaissance aircraft, such as small instantaneous bandwidth and low sensitivity. According to the Nyquist sampling theorem [3], high sampling rates of ADC can provide ideal detection bandwidth. However, achieving higher detection frequency resolution requires performing large-point FFT (exceeding 1024 points) [4]. The significant computational load resulting from this can negatively impact the real-time nature of signal detection, thereby affecting the performance of electronic reconnaissance aircraft.

In existing research on electronic reconnaissance aircraft, achieving a balance between instantaneous detection bandwidth, detection frequency resolution, and detection time has been a focal point. These performance parameters determine the precision strike capability and rapid response maneuverability in electronic warfare, reflecting the important operational capability of electronic warfare. In order to reduce the impact of the significant computational load caused by large-point FFT on real-time signal detection, many studies have introduced high-speed monobit ADCs and designed monobit electronic reconnaissance receivers. Monobit Discrete Fourier Transform (DFT) can avoid multiplication operations, thus speeding up the computation. Some researchers designed a constant iteration architecture without using multipliers, which efficiently implements pipeline DFT computation and achieves higher real-time performance [5]. And some researchers gave a new method to replace the discrete Fourier transform for monobit receivers by using dynamic twiddle factors based on the split-radix fast Fourier transform (SRFFT) to optimize performance of monobit receivers [6].

However, the cost of this high performance is that it only retains the frequency and phase information of the signal while completely discarding the signal amplitude information, making it unsuitable for scenarios that require detection of signal amplitude or multiple carrier radar signals. Therefore, some researches have focused on optimizing multi-bit FFT architectures to improve the performance of electronic reconnaissance aircraft. For example, a new type of digital electronic reconnaissance aircraft with a detected instantaneous bandwidth of 675 MHz and a detection time of 2 us is implemented by using multi-bit high-speed ADCs and FPGA to perform small-point (512 points) FFT on the signal [7]. And through a combined FFT structure, a multi-signal detection environment for four carrier signals with different frequency is achieved on FPGA [8].

Compared to previous works, this paper utilizes the new high-performance hardware platform RFSoC and designs an 8-channel parallel data processing structure to perform a 4096-point large-point FFT. Under the premise of instantaneous detection bandwidth of 2 GHz and detection frequency resolution of 1 MHz, the signal detection time is reduced from 25 us to approximately 3 us, and it also has the capability to detect multiple carrier frequencies of continuous wave radar. These improvements enhance the performance of the electronic reconnaissance aircraft in multiple aspects and provide a strong foundation for localization [9], interference, deception, and other strike tactics. The content of this paper is organized as follows: Section II presents a detailed description of the implementation model and principles, and Section III exhibits the simulation results and experimental results.

II. Implementation Model and Principles

A. System Model

Currently, the mainstream electronic reconnaissance aircraft mainly consist of RF front-end circuits, high-speed ADCs, and processing units. The implementation in this paper

is based on the system model shown in Fig. 1. The weak RF Signal received by the antenna has a more suitable Signal-to-Noise Ratio (SNR) after passing through the automatic gain control (AGC) module. After frequency mixing, the down-converted signal is split by a power divider, with one part output to the detector module for calculating pulse parameters and acting as an indication signal for effective carrier sampling. The other is directly output to the processing core RFSoC for computing other parameters.

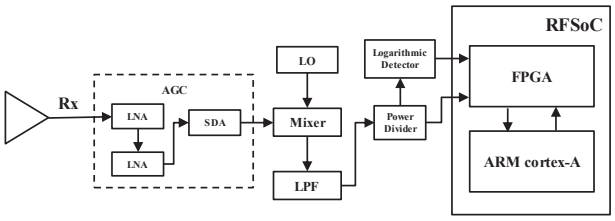

Fig. 1. Digital EW receiver system model

RFSoC is a high-performance System-on-Chip (SoC) developed by Xilinx, which integrates RF and digital signal processing capabilities into a single chip. It integrates multiple high-speed ADCs with sampling rates up to 4.096 GSPS, ARM Cortex-A53 processors, Field-Programmable Gate Array (FPGA), and rich memory resources and peripheral interfaces, providing high-performance RF and digital signal processing capabilities [10].

Despite RFSoC has high-speed RF and digital signal processing capabilities, the limitation of FPGA operating clock frequency still poses challenges to high-performance real-time systems such as electronic reconnaissance aircraft, especially in the implementation of FFT algorithms. For instance, considering the RFSoC ADC sampling frequency of 4 GHz and FPGA clock frequency of 500 MHz, to achieve a frequency resolution of 1 MHz, it requires performing a 4096-point FFT on the sampled digital signal. For conventional FFT implementations, even with the use of pipelined FFT processing, significant time overhead can still be encountered, which could be detrimental to real-time signal detection.

To address this issue, we propose an optimization strategy, which involves using an 8-way parallel 512-point pipelined FFT to achieve a 4096-point FFT. This approach not only leverages the advantages of FPGA parallel computation but also considers the characteristics of RFSoC analog-to-digital conversion signal transmission. Specifically, to match the ADC sampling rate with the FPGA clock frequency, the RFSoC internally combines 8 consecutive 16-bit samples into a single 128-bit data stream, achieving real-time serial-to-parallel data conversion. This process provides the necessary parallel data foundation for implementing the 8-channel parallel FFT algorithm.

B. Principle of 8-Channel Parallel FFT

The Discrete Fourier Transform can obtain the frequency spectrum of a discrete-time signal, allowing for the analysis of the signal's characteristics in the frequency domain. Define $x(n)$ be the time sequence of length N obtained through continuous sampling by the ADC. The DFT is defined as follows:

$$X(k) = DFT[x(n)] = \sum_{n=0}^{N-1} x(n) W_N^{nk},\ k = 0,1,\dots N-1 \quad (1)$$

Where, $W_N^{nk} = e^{-j\frac{2\pi nk}{N}}$ is the twiddle factor. From (1), it can be observed that each N-point DFT computation requires N^2 complex multiplications and $N(N-1)$ complex additions. As N increases, the computational complexity will increase significantly [11]. The twiddle factor possesses several properties:

- Periodicity: $W_N^{n(N-k)} = W_N^{k(N-n)} = W_N^{-nk}$ (2)
- Symmetry: $W_N^{nk+N/2} = -W_N^{nk} = \left(W_N^{kn}\right)^*$ (3)
- Reducibility: $W_N^{nk} = W_{mN}^{nmk}$ (4)

Simultaneously, based on the RFSoC's sampling data transmission format, the input time sequence $x(n)$ is divided into eight groups: $x(8m)$, $x(8m+1)$, $x(8m+2)$, $x(8m+3)$, $x(8m+4)$, $x(8m+5)$, $x(8m+6)$, $x(8m+7)$. According to (2), (3), and (4), formula (1) can be represented as follows:

$$\begin{aligned} X(k) = {} & \sum_{m=0}^{\frac{N}{8}-1} x(8m) W_{\frac{N}{8}}^{mk} + W_N^k \sum_{m=0}^{\frac{N}{8}-1} x(8m+1) W_{\frac{N}{8}}^{mk} \\ & + W_N^{2k} \sum_{m=0}^{\frac{N}{8}-1} x(8m+2) W_{\frac{N}{8}}^{mk} + W_N^{3k} \sum_{m=0}^{\frac{N}{8}-1} x(8m+3) W_{\frac{N}{8}}^{mk} \\ & + W_N^{4k} \sum_{m=0}^{\frac{N}{8}-1} x(8m+4) W_{\frac{N}{8}}^{mk} + W_N^{5k} \sum_{m=0}^{\frac{N}{8}-1} x(8m+5) W_{\frac{N}{8}}^{mk} \\ & + W_N^{6k} \sum_{m=0}^{\frac{N}{8}-1} x(8m+6) W_{\frac{N}{8}}^{mk} + W_N^{7k} \sum_{m=0}^{\frac{N}{8}-1} x(8m+7) W_{\frac{N}{8}}^{mk} \\ & m = 0,1,\dots N/8-1 \end{aligned} \quad (5)$$

From (5), it can be observed that the N-point FFT result of the continuous-time sequence can be computed using the N/8-point FFT results of the 8 decimated sequences. Let the 8 results be: $F_0(k)$, $F_1(k)$, $F_2(k)$, $F_3(k)$, $F_4(k)$, $F_5(k)$, $F_6(k)$ and $F_7(k)$. Additionally, by letting $a = \frac{\sqrt{2}}{2}(1+j)$ and $b = \frac{\sqrt{2}}{2}(1-j)$, combined with the properties of the twiddle factor W_N^{nk}, the complete N-point FFT results can be obtained:

$$\begin{aligned} X(k) = {} & F_0(k) + F_1(k)W_N^k + F_2(k)W_N^{2k} + F_3(k)W_N^{3k} + \\ & F_4(k)W_N^{4k} + F_5(k)W_N^{5k} + F_6(k)W_N^{6k} + F_7(k)W_N^{7k} \\ X(k+N/8) = {} & F_0(k) + bF_1(k)W_N^k - jF_2(k)W_N^{2k} - aF_3(k)W_N^{3k} - \\ & F_4(k)W_N^{4k} - bF_5(k)W_N^{5k} + jF_6(k)W_N^{6k} + aF_7(k)W_N^{7k} \\ X(k+2N/8) = {} & F_0(k) - jF_1(k)W_N^k - F_2(k)W_N^{2k} + jF_3(k)W_N^{3k} + \\ & F_4(k)W_N^{4k} - jF_5(k)W_N^{5k} - F_6(k)W_N^{6k} + jF_7(k)W_N^{7k} \\ X(k+3N/8) = {} & F_0(k) - aF_1(k)W_N^k + jF_2(k)W_N^{2k} + bF_3(k)W_N^{3k} - \\ & F_4(k)W_N^{4k} + aF_5(k)W_N^{5k} - jF_6(k)W_N^{6k} - bF_7(k)W_N^{7k} \\ X(k+4N/8) = {} & F_0(k) - F_1(k)W_N^k + F_2(k)W_N^{2k} - F_3(k)W_N^{3k} + \\ & F_4(k)W_N^{4k} - F_5(k)W_N^{5k} + F_6(k)W_N^{6k} - F_7(k)W_N^{7k} \\ X(k+5N/8) = {} & F_0(k) - bF_1(k)W_N^k - jF_2(k)W_N^{2k} + aF_3(k)W_N^{3k} - \\ & F_4(k)W_N^{4k} + bF_5(k)W_N^{5k} + jF_6(k)W_N^{6k} - aF_7(k)W_N^{7k} \\ X(k+6N/8) = {} & F_0(k) + jF_1(k)W_N^k - F_2(k)W_N^{2k} - jF_3(k)W_N^{3k} + \\ & F_4(k)W_N^{4k} + jF_5(k)W_N^{5k} - F_6(k)W_N^{6k} - jF_7(k)W_N^{7k} \\ X(k+7N/8) = {} & F_0(k) + aF_1(k)W_N^k + jF_2(k)W_N^{2k} - bF_3(k)W_N^{3k} - \\ & F_4(k)W_N^{4k} - aF_5(k)W_N^{5k} - jF_6(k)W_N^{6k} + bF_7(k)W_N^{7k} \\ & k = 0,1,\dots N/8-1 \end{aligned} \quad (6)$$

C. RFSoC Algorithm Model

The algorithm implementation is mainly based on the parallel processing capability of FPGA, the high-speed ADC data parallel transmission format in RFSoC and the computational capability of ARM Cortex-A53 processor. Firstly, the data conversion module converts the sampled 16-bit serial data into 128-bit parallel data without delay, allowing N-point digital signals to be transmitted within *N*/8 clock cycles. The 128-bit data is divided into eight groups and undergoes *N*/8-point pipelined FFT computation, which effectively minimizes the FFT calculation latency. Meanwhile, the address control module controls the output of complex twiddle factors stored in BRAM according to specific logic. These twiddle factors and the complex results obtained from the multi-channel parallel FFT, are processed by the butterfly operation module and serially output the N-point FFT computation results with a certain timing. The N-point complex results are stored in BRAM and later processed by the ARM processor for peak detection, amplitude conversion, and other subsequent calculations. The overall algorithm model implemented in RFSoC is illustrated in Fig. 2.

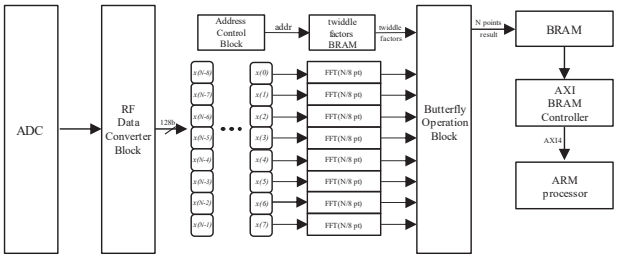

Fig. 2. Parallel FFT algorithm model based on RFSoC

This RFSoC-based parallel FFT scheme offers significant advantages over conventional serial FFT or other parallel FFT schemes. Compared to serial FFT, the RFSoC-based parallel FFT not only greatly reduces the transmission time of radar signal sampling data but also reduces the computational complexity by using a parallel FFT structure, thereby saving considerable time in complex calculations. Compared to other parallel FFT implementations, the RFSoC allows seamless and real-time serial-to-parallel conversion of high-speed sampled data, directly transmitting data with a 128-bit high bit width. This capability enables the FPGA to read the data within a single clock cycle, thereby shortening the data transmission time. This optimization significantly reduces the time overhead, leading to a remarkable improvement in FFT computation speed and enhancing the performance of electronic reconnaissance aircraft.

III. Simulation and Experimental Results

A. Simulation Results

To further validate the feasibility of the proposed approach, the main components of the algorithm were simulated in Matlab. Initially, a continuous wave radar signal with a frequency of 100 MHz, superimposed with Gaussian white noise, was generated and sampled with a length of 4096 points. Then, the signal was evenly sub-sampled to obtain eight sets of 512-point sub-sequences. Subsequently, a parallel FFT processing structure was designed, and the sub-sampled sequences were input to this structure to obtain eight sets of 512-point complex result sequences. Finally, the complex sequences underwent butterfly operations to generate the frequency-domain representation of the time-domain signal. A comparison of the results obtained from normal serial FFT and parallel FFT is shown in Fig. 3. It can be observed that the frequency-domain information obtained from both serial and parallel FFT computations is correct and consistent, demonstrating the feasibility of the parallel FFT algorithm.

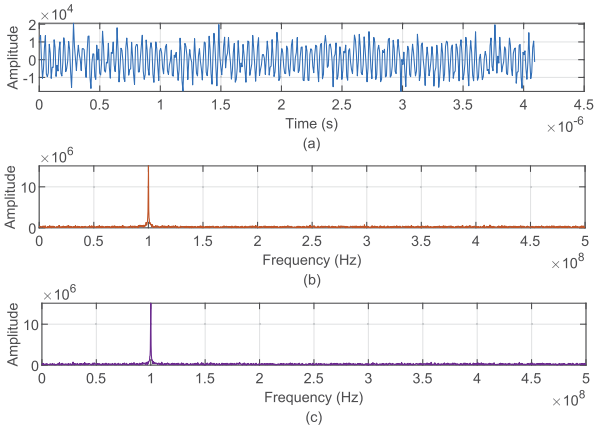

Fig. 3. (a) The time domain diagram of the continuous wave radar signal with a frequency of 100 MHz superimposed with Gaussian white noise; (b) The serial FFT result; (c) The parallel FFT result.

B. Experimental Results

We simulated the radar signal source using a signal generator and transmitted the signal into the atmosphere through a planar spiral antenna. At a distance of one meter from the transmitting antenna, a receiving wideband dual-ridged horn antenna, the electronic reconnaissance system, and the host were placed. The experimental setup is illustrated in Fig. 4.

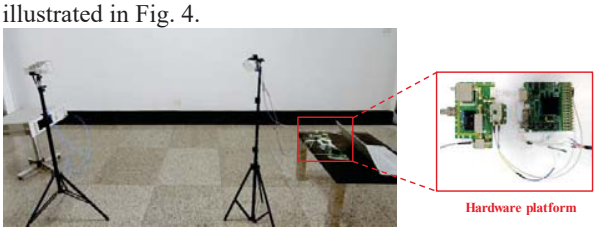

Fig. 4. Experimental setup

After the hardware system completed the signal detection, the detection results were transmitted to the host via the JTAG interface, so that the Integrated Logic Analyzer (ILA) tool of Vivado can be used to capture multiple sets of data, including the sampled digital signals and FFT computation results. Finally, the captured data was exported to Matlab for system analysis. The time interval between the first clock cycle of transmitting digital signals and the last clock cycle of outputting FFT results is defined as the radar signal detection time.

After extracting the valid portion, the experimental results obtained with a transmission frequency of 2950 MHz and an amplitude of -45 dBm are shown in Fig. 5. To ensure the reliability of the experimental results, multiple measurements were performed by varying the transmission signal parameters with the frequency ranging in 2 to 4 GHz and the amplitude ranging in -50 to -40 dBm. Specific experimental parameters and results are presented in TABLE I.

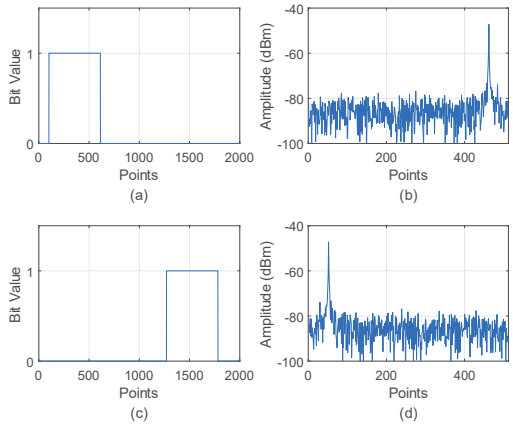

Fig. 5. (a) The FFT input data validity signal; (b) Results of the second set in parallel FFT; (c) The FFT output data validity signal; (d) Results of the seventh set in parallel FFT.

TABLE I. EXPERIMENTAL PARAMETERS AND RESULTS

Transmission		**Reception**		
Frequency (MHz)	***Amplitude (dBm)***	***Frequency (MHz)***	***Amplitude (dBm)***	***Time (us)***
2350	-50	2350	-53	3.3
2650	-48	2651	-49	3.3
2950	-45	2950	-46	3.3
3250	-43	3250	-43	3.3
3550	-40	3549	-40	3.3

The signal detection time can be calculated to be approximately 3.3 us, based on the difference in the number of points between Fig. 5(a) and Fig. 5(c), with the FPGA clock frequency set at 500 MHz. From Fig. 5(b) and Fig. 5(d), it can be observed that the frequency domain peaks appear in the butterfly operation results of the second and seventh FFTs, corresponding to the actual frequency and its mirror image in the Sub-Nyquist domain, respectively. Considering the local oscillator frequency as 2 GHz, the corrected actual frequency is calculated to be 2950 MHz, and the actual amplitude is approximately -46 dBm, which is consistent with the transmitted signal.

C. Resource Utilization of FPGA

The FPGA resource utilization for the proposed design is presented in TABLE II.

TABLE II. RESOURCE UTILIZATION OF FPGA DESIGN

Resources	**Used**
LUT	8956 (2.10%)
BRAM	43 (3.98%)
DSP	104 (2.43%)

IV. CONCLUSION

This paper proposes a real-time radar signal detection method based on RFSoC, enabling signal detection in approximately 3 us with an instantaneous bandwidth of 2 GHz and a frequency resolution of 1 MHz. This method also provides the capability to detect multiple carrier frequencies in radar signals. The performance of the proposed method is validated through simulations and experiments in real-world scenarios, ensuring the reliability of the system. For modern electronic warfare, the speed and accuracy of radar signal detection are crucial, making the method of this paper highly valuable for the design of next-generation electronic reconnaissance aircraft. In future work, we will continue to optimize the radar signal detection structure based on RFSoC, aiming to further reduce system resource consumption, improve the performance of electronic reconnaissance aircraft, and make the system adapt to more radar signal detection environments.

ACKNOWLEDGMENT

This work is supported in part by the National Key R&D Program of China (No. 2022YFE0112600), the Zhejiang Jianbing Plan (2022C01028), the NSFC (U21A20456, 62271444), the Zhejiang Provincial NSFC (LZ23F010007), the Fundamental Research Funds for Central Universities (226-2022-00107 ， 226-2023-00111), the ZJU Qizhen Scholar Foundation and the 5G Open Laboratory of Hangzhou Future Sci-Tech City.

REFERENCES

[1] Z. Zhang, Z. Shi, and Y. Gu, “Ziv-Zakai Bound for DOAs Estimation,” *IEEE Trans. Signal Process.*, vol. 71, pp. 136–149, 2023.

[2] F. A. Butt and M. Jalil, “An overview of electronic warfare in radar systems,” in *2013 The International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE)*, Konya, Turkey: IEEE, May 2013, pp. 213–217.

[3] C. Zhou, Y. Gu, Z. Shi, and M. Haardt, “Structured Nyquist Correlation Reconstruction for DOA Estimation With Sparse Arrays,” *IEEE Trans. Signal Process.*, vol. 71, pp. 1849–1862, 2023.

[4] T. Siu, C.-W. Sham, and F. C. M. Lau, “Operating frequency improvement on FPGA implementation of a pipeline large-FFT processor,” in *2017 19th International Conference on Advanced Communication Technology (ICACT)*, Feb. 2017, pp. 5–9.

[5] P. Ji, H. Lv, Q. Shi, and N. Yuan, “Design of A High Performance Monobit DFT Based on FPGA and 1-Bit Samplers,” in *2020 7th International Conference on Information Science and Control Engineering (ICISCE)*, Changsha, China: IEEE, Dec. 2020, pp. 2375–2379.

[6] P. Ji, Q. Shi, and N. Yuan, “Dynamic Twiddle Factors Split-Radix Fast Fourier Transform for Monobit Receivers,” in *2020 IEEE International Conference on Signal Processing, Communications and Computing (ICSPCC)*, Macau, China: IEEE, Aug. 2020, pp. 1–4.

[7] D. Gupta, A. A. Bazil Raj, and A. Kulkarni, “Multi-Bit Digital Receiver Design For Radar Signature Estimation,” in *2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, Bangalore, India: IEEE, May 2018, pp. 1072–1075..

[8] A. Orduyilmaz, M. Ispir, M. Serin, and M. Efe, “Ultra Wideband Spectrum Sensing for Cognitive Electronic Warfare Applications,” in *2019 IEEE Radar Conference (RadarConf)*, Boston, MA, USA: IEEE, Apr. 2019, pp. 1–6.

[9] H. Zheng, Z. Shi, C. Zhou, M. Haardt, and J. Chen, “Coupled Coarray Tensor CPD for DOA Estimation With Coprime L-Shaped Array,” *IEEE Signal Process. Lett.*, vol. 28, pp. 1545–1549, 2021.

[10] F. Michalak, W. Zabołotny, Ł. Podkalicki, M. Malanowski, M. Piasecki, and K. Kulpa, “Universal RFSoC-based Signal Recorder for Radar Applications,” in *2022 23rd International Radar Symposium (IRS)*, Sep. 2022, pp. 136–140.

[11] M. Sun, L. Tian, and D. Dai, “Radix-8 FFT processor design based on FPGA,” in *2012 5th International Congress on Image and Signal Processing*, Chongqing, Sichuan, China: IEEE, Oct. 2012, pp. 1453–1457.