同行专家业内评价意见书编号：20240854244

附件1

浙江工程师学院（浙江大学工程师学院）
同行专家业内评价意见书

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申报工程师职称专业类别（领域）：电子信息

浙江工程师学院（浙江大学工程师学院）制

2024年03月29日

一、个人申报

（一）基本情况【围绕《浙江工程师学院（浙江大学工程师学院）工程类专业学位研究生工程师职称评审参考指标》，结合该专业类别(领域)工程师职称评审相关标准，举例说明】

1. 对本专业基础理论知识和专业技术知识掌握情况

这些年来，我致力于对本专业理论与人工智能的结合，并不断实践，以提升我的专业技术能力。

在基础理论知识方面，我系统学习了电路理论、信号与系统、数字逻辑设计、模拟电路设计、微电子学、通信原理等核心课程。这些课程不仅为我后续的专业发展奠定了坚实的理论基础，也使我在理解复杂电子系统的设计与分析方面具有了较强的能力。此外，我还学习了最新的边缘计算的相关知识信息，以保持我的专业知识的前沿性。在学习期间我发表了两篇论文和申请了一篇专利。

在专业技术知识与技能方面，我有丰富的实践经验。我参与了多个与电子信息工程相关的项目，如智能传感器开发、嵌入式系统设计、无线通信系统的优化等。在这些项目中，我不仅应用了我所学的理论知识，解决了实际工程问题，还通过团队合作，提升了我的项目管理能力和跨领域协作能力。特别是在嵌入式系统设计项目中，我负责整个系统的设计与实现，这个过程中深入学习了微控制器编程、硬件设计以及系统集成，进一步增强了我的技术实践能力。

2. 工程实践的经历

2021年3月----2021年9月　　南京赫伯纳电子科技有限公司

2022年11月----2023年7月　　浙江运达风电股份有限公司

3. 在实际工作中综合运用所学知识解决复杂工程问题的案例

在国家积极推动能源结构转型背景下，电动汽车等新能源产业得到了迅速发展。锂离子电池以其高能量密度、长使用寿命以及显著的标称电压和容量优势，在支持电动汽车需求增长方面发挥着关键作用。荷电状态（State of Charge，SOC）作为锂离子电池的一个核心参数，不仅代表了电池的可用容量，还确保电动汽车系统的安全可靠运行。在电池管理系统中，准确估计 SOC 是至关重要的。近年来，随着人工智能技术的飞速发展和广泛应用， SOC 的估计方法也逐渐转向以数据为驱动的新方法。基于这一背景，我们开展了一项通过人工智能算法估计锂电池SOC的项目：

项目技术的主要难点在于两个方面：第一，如何准确的估计电池SOC；第二，如何降低人工智能模型所耗费的算力和存储资源。为了攻克这些难题，我们采取了以下解决方案：

首先提出了一种多尺度 CNN-LSTM 融合网络，该网络考虑到了传感数据的频变信息，对特征数据进行分组卷积，有效提升了SOC的估计精度。考虑到电池内部化学反应的复杂性及其所呈现的平台效应，完全依赖数据驱动的方法可能存在不足。因此，我们在神经网络的输出层结合了无迹卡尔曼滤波（Unscented Kalman Filter，UKF）技术，以增强模型的鲁棒性并减少随机误差。通过实验验证，这种结合了 CNN-LSTM 和 UKF 的方法不仅提高了 SOC 估计的准确性，而且展现了其泛化能力。

考虑到电池通常用于资源受限的设备中，而人工智能算法需要大量的存储和计算资源，在所提模型的基础上，采用 Group Lasso 正则化来实现模型的稀疏化，然后通过结构化剪枝技术简化模型结构，有效降低了网络的复杂度。进一步地，为了减少浮点运算的复杂性，对模型采用了静态和动态混合量化策略，分别适用于 CNN 和 LSTM。处理后的模型显著减少了对存储的需求，并提高了运行效率，从而更适合于资源有限的环境。

项目实施后的实际效果与成果显著。基于多尺度 CNN-LSTM
结合UKF方法在估计SOC方面保持了极高的精度。其估计平均绝对误差、均方根误差和最大误差分别为 0.37%、 0.42% 和 0.80%。而传统LSTM
网络估计的均绝对误差、均方根误差和最大误差分别为 1.34%、 1.53% 和
4.20%。相比于传统的LSTM网络， CNN-LSTM-
UKF能够得到更小的SOC估计误差。此外，通过轻量化算法对 CNN-LSTM-UKF
模型资源占用带来了显著的改进。原模型的大小为
102.1KB，经过轻量化处理后降至3.4KB，实现了约 30
倍的存储资源节约。同样，推理时间也从 3.71ms 显著减少至 0.51ms，计算速度提升了约7倍。综合来看，这种轻量化处理在降低模型的复杂性和资源消耗的同时，有效的维持了较高的估计精度，在高效率与高精度之间的保持卓越的平衡。项目为锂电池SOC估计供了可靠的技术方案，促进了电池能源行业的发展。
综上所述，本项目通过跨学科合作和技术革新，在锂电池SOC估计方面取得了显著成效。未来，随着技术的不断成熟和推广应用，我们有理由相信，它将在更复杂的电池应用场景产生深远的影响，改善边缘端部署人工智能算法的现状，助力工业智能化改革，为新能源领域做出重要贡献。

（二）取得的业绩（代表作）【限填3项，须提交证明原件（包括发表的论文、出版的著作、专利证书、获奖证书、科技项目立项文件或合同、企业证明等）供核实，并提供复印件一份】					
1. 公开成果代表作【论文发表、专利成果、软件著作权、标准规范与行业工法制定、著作编写、科技成果获奖、学位论文等】					
成果名称	成果类别 [含论文、授权专利（含发明专利申请）、软件著作权、标准、工法、著作、获奖、学位论文等]	发表时间/授权或申请时间等	刊物名称/专利授权或申请号等	本人排名/总人数	备注
配电网设备数据采集装置及配电网设备ID自动分配方法	发明专利申请	2022年08月24日	申请号：202211020631.0	1/6	
A Novel Data Acquisition Equipment for Distribution Systems Based on FFT Single-peak Interpolation Algorithm	会议论文	2023年09月20日	China Automation Congress 2023	1/3	
A Fast Power Harmonic Detection Framework based on FPGA	会议论文	2024年02月08日	the 36th Chinese Control and Decision Conference	1/3	

2. 其他代表作【主持或参与的课题研究项目、科技成果应用转化推广、企业技术难题解决方案、自主研发设计的产品或样机、技术报告、设计图纸、软课题研究报告、可行性研究报告、规划设计方案、施工或调试报告、工程实验、技术培训教材、推动行业发展中发挥的作用及取得的经济社会效益等】

（三）在校期间课程、专业实践训练及学位论文相关情况	
课程成绩情况	按课程学分核算的平均成绩： 83 分
专业实践训练时间及考核情况(具有三年及以上工作经历的不作要求)	累计时间： 1 年（要求1年及以上） 考核成绩： 82 分（要求80分及以上）
本人承诺	
个人声明：本人上述所填资料均为真实有效，如有虚假，愿承担一切责任，特此声明！ **申报人签名：** 李健	

浙 江 大 学 研 究 生 院

攻读硕士学位研究生成绩表

学号：22160040	姓名：李健	性别：男	学院：工程师学院	专业：电子信息	学制：2.5年
毕业时最低应获：24.0学分	已获得：28.0学分			入学年月：2021-09	毕业年月：2024-03
学位证书号：1033532024602137			毕业证书号：103351202402600363		授予学位：电子信息硕士

学习时间	课程名称	备注	学分	成绩	课程性质	学习时间	课程名称	备注	学分	成绩	课程性质
2021-2022学年秋季学期	储能原理		2.0	85	专业学位课	2021-2022学年春季学期	储能器件与装备		2.0	91	专业学位课
2021-2022学年秋季学期	储能材料		2.0	85	专业学位课	2021-2022学年春季学期	数学建模		2.0	86	专业选修课
2021-2022学年秋季学期	信息安全导论		2.0	87	专业选修课	2021-2022学年春季学期	自然辩证法概论		1.0	77	公共学位课
2021-2022学年冬季学期	模式识别与人工智能		2.0	89	专业学位课	2021-2022学年夏季学期	储能系统及应用		2.0	88	专业学位课
2021-2022学年秋冬季学期	中国特色社会主义理论与实践研究		2.0	89	公共学位课	2021-2022学年夏季学期	研究生英语		2.0	70	公共学位课
2021-2022学年冬季学期	标准与知识产权		2.0	95	专业选修课	2022-2023学年秋季学期	创新创业实践训练		2.0	通过	跨专业课
2021-2022学年冬季学期	工程伦理		2.0	94	公共学位课	2023-2024学年秋季学期	研究生英语应用能力提升		2.0	76	公共学位课
2021-2022学年秋冬季学期	研究生论文写作指导		1.0	91	专业学位课						

说明：1. 研究生课程按三种方法计分：百分制，两级制（通过、不通过），五级制（优、良、中、及格、不及格）。

2. 备注中“*”表示重修课程。

学院成绩校核章：

成绩校核人：张梦依

打印日期：2024-04-02

22160040

二、日常表现考核评价及申报材料审核公示结果

日常表现考核评价	非定向生由德育导师考核评价、定向生由所在工作单位考核评价： ☑优秀　☐良好　☐合格　☐不合格 德育导师/定向生所在工作单位分管领导签字（公章）：　　年　月　日
申报材料审核公示	根据评审条件，工程师学院已对申报人员进行材料审核（学位课程成绩、专业实践训练时间及考核、学位论文、代表作等情况），并将符合要求的申报材料在学院网站公示不少于5个工作日，具体公示结果如下： ☐通过　☐不通过（具体原因：　　） 工程师学院教学管理办**公室**审核签字（公章）：　　年　月　日

(19)国家知识产权局

(12)发明专利申请

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(43)申请公布日 2022.12.20

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H04L 67/10(2022.01)
H04L 67/12(2022.01)
H04W 4/38(2018.01)

权利要求书2页 说明书5页 附图4页

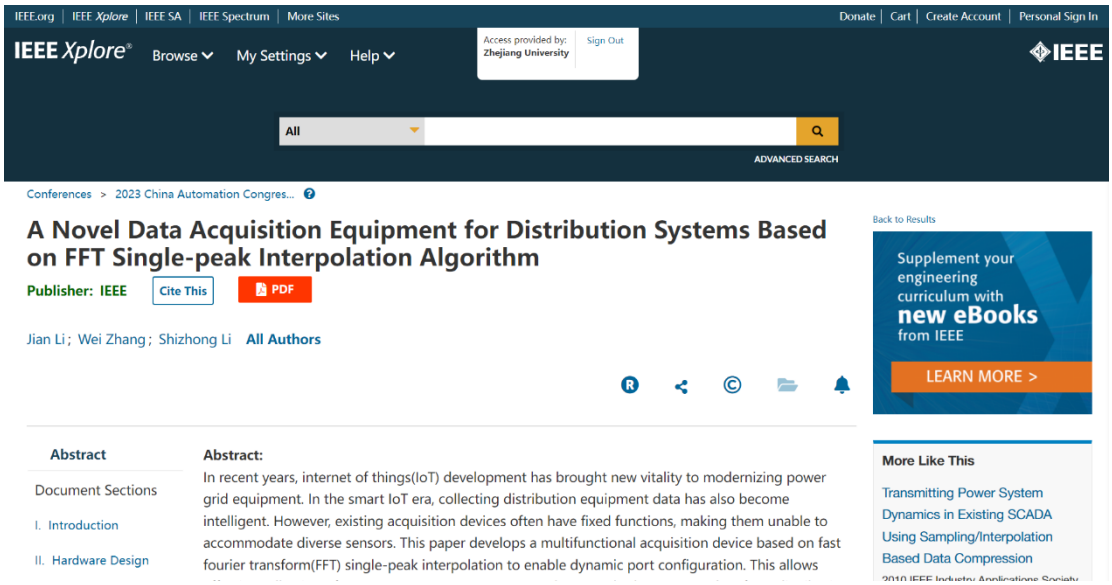
(54)发明名称

配电网设备数据采集装置及配电网设备ID自动分配方法

(57)摘要

本发明涉及电力数据采集技术领域，且公开了一种配电网设备数据采集装置及配电网设备ID自动分配方法，装置包括处理器模块和分别连接到所述处理器模块上的电源模块、RS485总线模块、SPI Flash存储模块、LED模块、UART模块，其中：所述UART模块用于与串口屏相连，实现人机交互，串口屏通过所述UART模块读取所述处理器模块的运行数据以及RS485总线模块采集的仪器仪表数据；串口屏通过所述UART模块下达指令给所述处理器模块，间接控制仪器仪表；所述RS485总线模块作为ModbusRTU主站协议，分别连接不同数量的仪器仪表，以实现对仪器仪表的数据采集与控制；减少了操作人员的重复劳动，同时减少了人工操作过程中出现的人为错误，使用方法灵活，提高了产品利用率，降低了生产成本。

CN 115499723 A



网址：https://ieeexplore.ieee.org/document/10451978

A Novel Data Acquisition Equipment for Distribution Systems Based on FFT Single-peak Interpolation Algorithm

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***Abstract*—In recent years, internet of things(IoT) development has brought new vitality to modernizing power grid equipment. In the smart IoT era, collecting distribution equipment data has also become intelligent. However, existing acquisition devices often have fixed functions, making them unable to accommodate diverse sensors. This paper develops a multifunctional acquisition device based on fast fourier transform(FFT) single-peak interpolation to enable dynamic port configuration. This allows effective collection of pressure, temperature, current, voltage, and other sensory data from distribution equipment. The device also enables real-time grid voltage harmonic calculation. Field testing showed the device maintained stability with good data upload rates under multiple sensor connections. The harmonic calculation accuracy met requirements, with an average 0.001% relative frequency error, 0.13% relative amplitude error, and 0.25° angular error.**

***Index Terms*—FFT, ARM, distribution system, interpolation algorithm**

I. Introduction

Recent IoT developments have created opportunities for smart grid advancement. Integrating massive sensing devices has accelerated the construction of intelligent electric power IoT [1]. Distribution grid equipment plays a critical role by collecting vital state information like voltage, current, temperature, and SF6 pressure to ensure smooth operation. Timely monitoring data access, transmission, and processing is essential for maintaining industrial IoT systems [2]. Significant research exists on distribution network data acquisition devices, including an adaptive IoT gateway with edge computing for configurable acquisition and multi-protocol transmission [3], and a microcontroller utility device for long-term voltage and frequency measurements, with computer data storage [4].

The waveform of the power grid is one of the most important monitoring data points. Deviations in the waveform shape and amplitude characteristics can compromise the safety of the power system [5]. Therefore, analysis of the power waveform is particularly crucial.There are many methods for harmonic analysis. [6] accomplishes harmonic extraction using wavelet transform. [7] analyzes harmonics through FFT. In recent years, with the rise of artificial intelligence algorithms, many scholars have also applied neural networks to the field of harmonic analysis [8]–[10]. These algorithms are usually deployed on MCUs, DSPs, or higher performance processors.

In this paper, a reconfigurable power data acquisition device for power distribution equipment is developed, and a smart grid digitization solution is proposed based on the data acquisition device, as shown in Fig.1. This solution realizes full-range sensing of different power cabinets and provides support for cloud service data analysis. The dynamic configuration function and one-to-many acquisition function of the data acquisition device solve the problems of traditional power data acquisition devices, including scene limitations and low utilization of device resources. A variable window FFT single-peak interpolation algorithm is deployed on the data acquisition device, enabling quick and low-error calculation of grid harmonics.The main contributions of this paper are summarized as follows.

1) In this paper, the designed power data acquisition device differs from traditional ones by introducing the concept of port reconfiguration. The reconfiguration is initialized according to the Json configuration file in the memory chip when the system is reset. The Json file is generated and imported by the host computer. This scheme can greatly improve the user's operation efficiency and further enhance grid instrumentation intelligent.
2) A variable sliding window FFT single peak interpolation algorithm is proposed. It uses the sliding window to calculate each harmonic in turn, which can reduce memory occupation. The size of the sliding window can be specified so that the window can be minimized to reduce the computational pressure of the system. Finally, the algorithm is deployed in the system.

II. Hardware design

In this section, we provide a detailed description of the hardware design for the data acquisition device. The overall hardware architecture is illustrated in Fig.2. As shown, the device offers a variety of communication interfaces that are

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A Fast Power Harmonic Detection Framework based on FPGA

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***Abstract*—With the rise of modern electronics and technology, various non-linear loads have become integral to our daily lives. The resulting distortion of current and voltage waveforms in the power grid has the potential to trigger malfunctions in electrical components, affecting the functionality and sustainability of the power system. Calculating accurate harmonic content, considering harmonic frequency, amplitude, and phase angle, is a crucial step in addressing harmonic issues. This research article introduces an embedded systems-tailored power harmonic detection method based on the Fast Fourier Transform (FFT) algorithm. This innovative approach significantly enhances the computational precision of FFT. Implemented on the ZYNQ-7000 system on chip, it demonstrates a notable decrease in relative error compared to default data. Furthermore, the operational speed surpasses that of conventional microcontroller devices by 33 times, marking it as a powerful alternative for efficient power harmonic detection.**

***Index Terms*—ARM, FFT, FPGA, harmonic, smart grid**

I. Introduction

As recent years have seen increasing dependency on electrical energy, society faces an insatiable demand that challenges the capacity of less efficient energy sources [1]. This scenario highlights an indisputable global demand for abundant, cost-effective, and accessible energy provisions. Undoubtedly, power distribution rooms serve as the lifeblood of urban landscapes, discreetly located in diverse settings, from expansive commercial squares to individual buildings [2]. These locations emphasize the vital role of power grids within them, with their performance significantly influencing every aspect of daily life. As such, the quality of these power grids is not merely a necessity but a crucial element in ensuring the steady rhythm of societal functioning.

Electric power undergoes various objective conditions during production and transmission, resulting in the deformation of power signal waves. This deformation gives rise to power quality issues. On one hand, the extensive use of power electronic equipment in enterprises generates numerous harmonics, causing deviations in the waveform and amplitude characteristics of electric energy. This, in turn, poses a threat to the safety of the power system [3]. On the other hand, as advanced instruments and equipment are increasingly employed in industrial production for state monitoring [4], [5], the demand for power waveform quality is also on the rise.

There are many methods for harmonic analysis. For example, Gu *et al.* [6] accomplishes harmonic extraction by wavelet transform, and Shao *et al.* [7] analyses harmonics by fast Fourier Transform (FFT). In recent years, with the rise of artificial intelligence algorithms, many scholars also apply neural networks in the field of harmonic analysis [8]–[10], and these algorithms are usually deployed on microcontroller units (MCU), digital signal processing (DSP), or higher-performance processors. As these processors execute instructions serially, harmonic detection can be slow. Therefore, we propose a fast power harmonic detection framework (FPHDFF) based on a field-programmable gate array (FPGA) to fully leverage parallel processing advantages. The main contributions of this paper are summarized as follows.

1) This paper presents a fast power harmonic detection framework designed for swiftly detecting the amplitude, frequency, and phase of harmonics in power grids. The framework enhances the conventional FFT algorithm by incorporating interpolation calculations to effectively address the issue of non-coinciding harmonic frequencies on the spectral lines. Additionally, a fixed-point scaling mechanism is introduced during the FFT computation, significantly accelerating the calculation process.

2) The proposed architecture outlined in this paper successfully deploys the FPHDFF on FPGA and conducts precision and speed assessments. FPDHFF not only maintains high accuracy but also significantly boosts processing speed.

II. Mathematical Model

The construction of mathematical models is an indispensable step in simulating and forecasting voltage changes. This component is integral to the entire procedure.

In the context of power systems, the ideal grid voltage can be represented as:

$$u(t) = \sqrt{2}U\sin(\omega t + \varphi), \tag{1}$$

$$\omega = 2\pi f, \tag{2}$$

where ω denotes the angular frequency, f is indicative of the industrial frequency which is quantitatively defined as 50 Hz, φ represents the initial phase, and U is a predefined constant possessing a value of 220V.

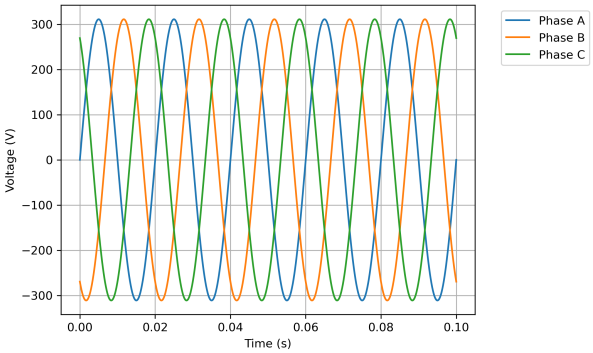

Fig. 1. Ideal three-phase voltage waveform.

Fig. 1 depicts the ideal three-phase voltages where the phases are 120° apart, each phase voltage represented by a pure sine wave without any harmonic components. In practical situations, such an ideal voltage doesn't exist. When sinusoidal voltages interact with nonlinear loads like rectifiers, variable frequency drives, and switch-mode power supplies, the fundamental currents undergo distortion, leading to the generation of harmonics. These distorted three-phase voltages are depicted in Fig. 2.

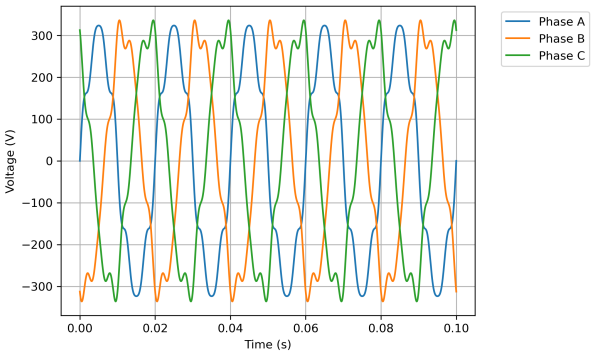

Fig. 2. Actual three-phase voltage waveform.

In the power system, harmonics refer to components in the Fourier series decomposition of a non-sinusoidal periodic waveform [11]. These components not only include those at the fundamental frequency of the power network but also consist of higher-frequency components, which are termed harmonics.

When no sinusoidal voltage with period T satisfies the Dirichlet condition, it can be decomposed by Fourier series as:

$$u(\omega t) = a_0 + \sum_{n=1}^{\infty}(a_n \cos(n\omega t) + b_n \sin(n\omega t)), \quad (3)$$

$$a_0 = \frac{1}{2\pi}\int_0^{2\pi} u(\omega t)d(\omega t), \quad (4)$$

$$a_n = \frac{1}{\pi}\int_0^{2\pi} u(\omega t)\cos(n\omega t)d(\omega t) \quad n = 1, 2, 3..., \quad (5)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} u(\omega t)\sin(n\omega t)d(\omega t) \quad n = 1, 2, 3.... \quad (6)$$

In Eqs. 5 and 6, the component corresponding to $n = 1$ is referred to as the fundamental, while the component for $n > 1$ is termed a harmonic. With increasing values of n, the count of harmonics also increases. Eq. 5 depicts an even number of terms, totaling $2n$ harmonics, whereas Eq. 6 represents an odd number of terms, summing up to $2n + 1$ harmonics.

Processing time-domain signals directly can be intricate, prompting the need for their transformation into the frequency domain for analysis. The Fast Fourier Transform (FFT) has become the predominant algorithm in the field of digital signal processing for this purpose [12].

A continuous signal, $x(t)$ is sampled with a sampling rate of F_s and a sample length of N, yielding the discrete sequence $x_n = (x_0, x_1, ..., x_{N-1})$. The FFT of this signal can be described as:

$$x(k) = \sum_{n=0}^{N/2-1} x(2n)W_N^{2nk} + \sum_{n=0}^{N/2-1} x(2n+1)W_N^{(2n+1)k}, \quad (7)$$

where, W represents the rotation factor, and $x(n)$ denotes the coefficient.

Each FFT operation is limited to transforming a finite length of time-domain data, requiring truncation of the signal in the time domain. When the truncated time length doesn't align as an integer multiple of the period (period truncation), it results in leakage within the intercepted signal. The use of window functions effectively mitigates spectrum leakage. Commonly employed window functions include the Hann window [13], Triangular window [14], and Rectangular window [15]. Among these, the Hann window effectively suppresses high-frequency interference, making it widely utilized in harmonic analysis. The time-domain expression of the Hann window is given by:

$$\omega(n) = \frac{1}{2}\left(1 - cos\left(\frac{2\pi(n-1)}{N}\right)\right), \quad (8)$$

given that a spectrum constitutes a discrete sequence, only the sampled points are observable, lacking representation of details between these discrete points. When the frequency components of a signal don't precisely align with the peaks of the spectrum, computation outcomes may exhibit biases, necessitating data fitting. The single-peak spectrum line interpolation algorithm offers advantages such as simplicity in computation and high efficiency. This paper employs the Hann window FFT single-peak spectrum line interpolation algorithm, outlined as follows:

$$f_k = frequency[X(k)] + \lambda\frac{F_s}{N}, \quad (9)$$

$$A_k = |X(k)|\frac{2\pi\lambda\left(1-\lambda^2\right)}{sin\left(\pi\lambda\right)}, \quad (10)$$

$$\varphi_k = angle[X(k)] - \pi\lambda(N-1)/N, \quad (11)$$

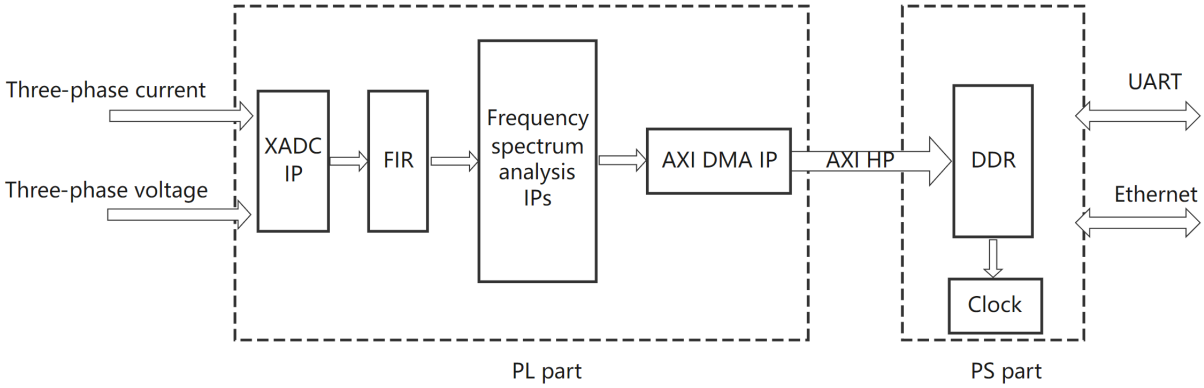

Fig. 3. The comprehensive design of the FPDHFF structure.

where $\lambda = (2\beta-1)/(\beta+1)$, $\beta = |X(k+1)|/|X(k)|$, $X(k)$ is the amplitude of the spectral line at point k, F_s is the sampling frequency, and N is the FFT length.

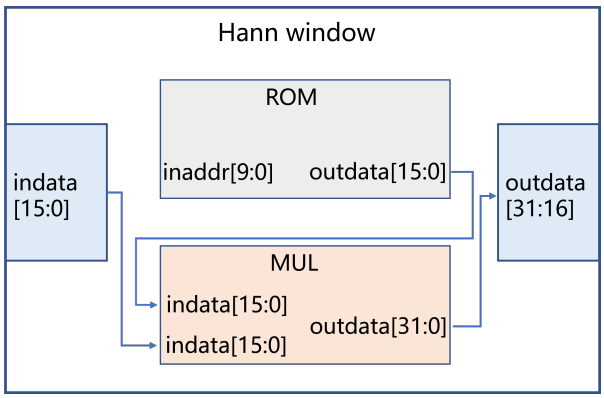

Fig. 4. The data format of the Hann window module.

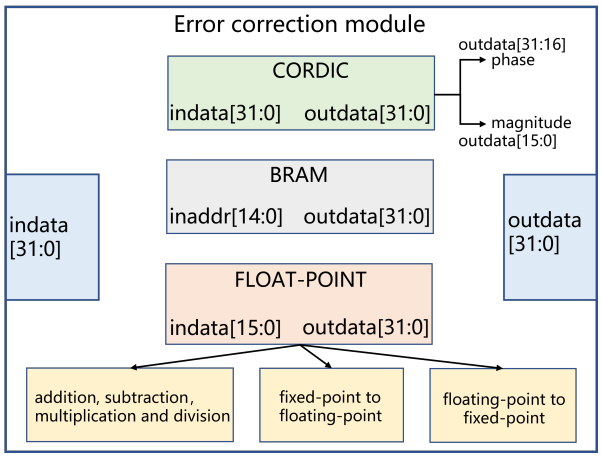

Fig. 5. The data format of the error correction module.

It's important to note that Eq. 9 represents the frequency correction equation, Eq. 10 represents the amplitude correction equation, and Eq. 11 represents the phase correction equation. Subsequent system design will revolve around these three equations.

III. Block Design

In this section, we present an elaborate system design overview, emphasizing our reliance on the Zynq-7020 processor by Xilinx. This processor stands out for its power efficiency and integration of a dual-core ARM Cortex-A9 along with an FPGA. This combination fulfills the dual demands of high performance in embedded systems and the requisite parallel processing capacity inherent to FPGAs. Presently, the Zynq-7020 finds extensive application across diverse domains of human life, including automotive, image processing, artificial intelligence, robotics, and more.

A. Overall Architecture

As previously mentioned, the Zynq-7020 comprises both an Arm processor (referred to as the PS part, encompassing the dual-core ARM Cortex-A9) and an FPGA (referred to as the PL part). We've designed these components separately. The overall architecture is illustrated in Fig. 3.

In Fig. 3, the three-phase current and voltage depict signals transmitted by the sensor. Within the PL part, modules such as the XADC data acquisition, filtering, spectrum analysis, and AXI DMA serve to process and perform logical operations on these signals. The spectrum analysis module comprises the Hann window module, FFT IP core, and a custom interpolation algorithm module. Results from the spectrum analysis module are directly conveyed to the DDR within the PS part through the AXI DMA IP core.

B. Design of Window Function

As already mentioned, the Hanning window is effective in reducing spectral ground leakage, the value of each point of the window function can be determined with the FFT length determined. These coefficients are stored by calling the Distributed memory generator IP core, and then the time domain data are multiplied with the coefficients separately and transferred to the FFT module. The input and output data formats of the Hann window module are shown in Fig. 4.

At the rising edge of every clock cycle, the module multiplies the input data with the ROM's output data, resulting in an output data length of 32 bits. To minimize communication bandwidth, data compression is implemented by truncating the $outdata[15:0]$ of the multiplier before its output.

C. Design of FFT Module

The official FFT IP core provided by Xilinx implements the FFT algorithm and has a visual design that allows the configuration of the FFT IP core related to your needs. The configuration table is shown in Table III-C.

TABLE I
CONFIGURATION OF KEY PARAMETERS FOR XFFT IP.

Properties	Configuration
FFT Channels	1
Implementation Structure	Streamline
FFT length	1024
Data Type	Fixed-point
Scaling Type	Scaled
Rounding mode	Truncation
Input data bit width	32bit
Phase factor bit width	32bit
Output sequence	Natural sequence

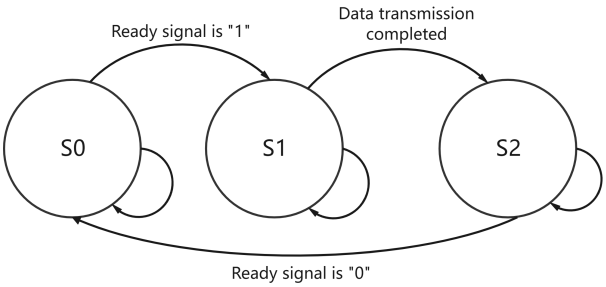

Fig. 6. PL part data sending program logic block diagram.

TABLE II
COMPARATIVE ANALYSIS OF COMPUTATION TIME.

	frequency	time
STM32-CMSIS	168MHz	10.87ms
ZYNQ-FPDHFF	100MHz	0.33ms

When conducting fixed-point FFT calculations, without appropriate scaling, overflow issues may arise in the results. Taking 16-bit fixed-point data as an example: the input data format is q15 (1 bit for the integer and 15 bits for the decimal), and without scaling, the output results in a format of 12-bit integer and 15-bit decimal. Hence, configuring a suitable scaling factor becomes crucial to prevent data overflow.

D. Design of Error Correction Module

The data output from the FFT module is a 32-bit complex binary fixed-point number, where the high sixteen bits of data represent the imaginary part and the complex numbers cannot

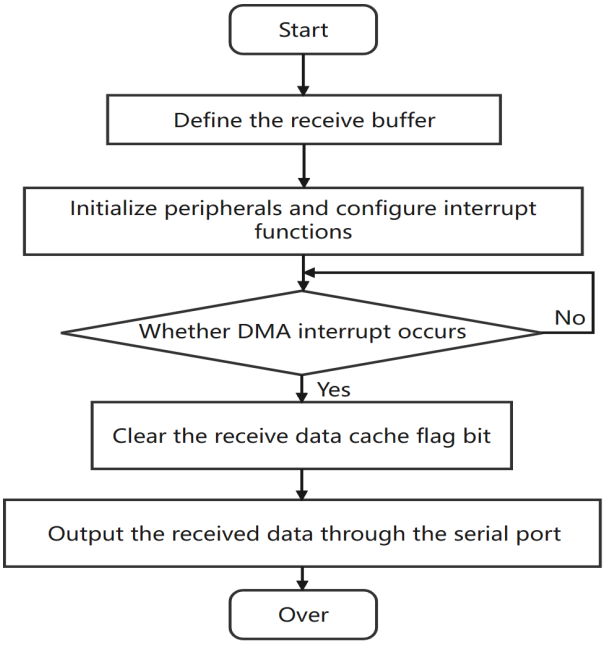

Fig. 7. PS part data reception program logic block diagram.

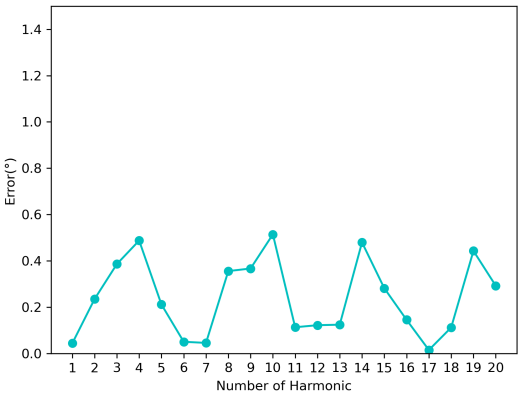

Fig. 8. Absolute error of harmonic phase angles.

be used directly. In order to facilitate subsequent calculations, the frequency domain data needs to be converted into phase and amplitude form. The input data of the CORDIC IP core is the output data of FFT, and the output data is 32-bit AXI Stream format, where the $outdata[31:16]$ represents the phase and the $outdata[15:0]$ bits represent the amplitude. We use two BRAM IPs to store the amplitude and phase. The data format is shown in Fig. 5.

The amplitude data type stored in BRAM is 1QN (q15 format) and the phase angle data type is 2QN (q14 format). Although the calculation speed of fixed-point data is fast, its calculation error is large, with only 2^n multiplication and division operations, in order to improve the accuracy of the calculation, the data need to be calculated in the form of

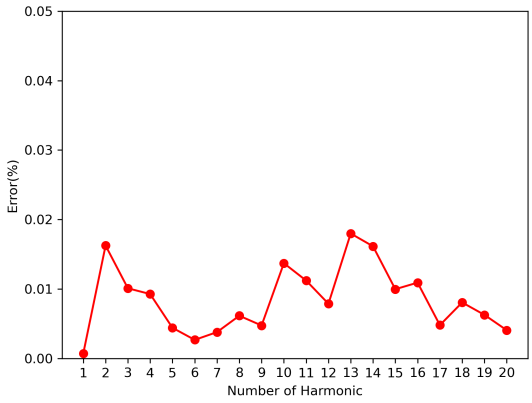

Fig. 9. Relative error of harmonic amplitudes.

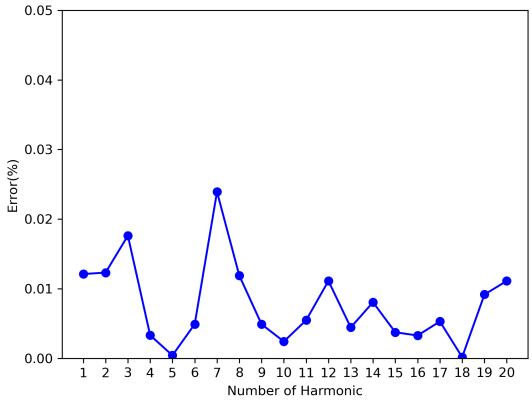

Fig. 10. Relative error of harmonic frequencies.

floating-point numbers, by using the Floating-point IP core for fixed-point to floating-point conversion and operation.

IV. Design of Data Transmission Program

PS can run more complex programs, and the results computed by PL are usually transferred to PS for use, so it is necessary to design a collaborative data transfer program between PL and PS.

A. Data Sending Program of PL

The code for PL to send data is designed based on AXI Stream's state machine, which functions to send the results to the PS. The state transition diagram is shown in Fig. 6.

PL data transmission is divided into 3 states, which are idle state (S0), send state (S1), and resume state (S2).

- S0: The Ready signal (host ready signal) is constantly detected, when the host is ready, then the Ready signal will become high at this time and set the t_valid signal to 1. The state jumps to S1.
- S1: Since it is detecting the 20th harmonic data, each harmonic contains three data of amplitude, frequency, and phase angle, only 60 data need to be sent in total. In S1, the sent data is counted and when the count value reaches 60, t_last signal is set to 1, and then the state jumps to S2.
- S2: Reset each signal, in order to prepare for the next data transmission. When the Ready signal remains valid, the count value will be cleared, and then the state jumps to S0.

B. Data Reception Program of PS

In this work, the PS is just a verification of the PL module's operation results, there is no other complicated design, in the following code, it is just repeatedly detecting whether the harmonic data sent by DMA IP is received or not, and then sending it to the upper computer through the serial port.

V. Results

To validate FPHDFF's performance, we conducted tests assessing both measurement accuracy and measurement time.

A. Accuracy Test

We simulated harmonic data from an electrical grid beneath a distribution room and conducted tests. This waveform encompasses harmonics up to the 20th order, comparing FPHDFF's accuracy in terms of magnitude, phase angle, and frequency.

From Fig. 10, it can be concluded that the average relative error of frequency calculated by FPDHFF is about 0.001%, the average error of angle is about 0.25°, and the average relative error of amplitude is about 0.13%.

The existence of errors, in addition to the inherent properties of FPHDFF, is also due to data truncation errors, rounding errors, and conversion errors between fixed-point and floating-point numbers, resulting in a certain bias in the final results. However, this detection accuracy can satisfy the index requirements of the instrumentation.

B. Speed Test of Measurement

Furthermore, in this section, we conducted a brief test on the computational speed of FPDHFF. As mentioned earlier, the FPDHFF architecture applied atop FPGA ensures notably fast computation due to its parallelism. We performed harmonic analysis speed tests on both the STM32 and ZYNQ platforms. For the STM32 platform, we utilized the CMSIS library, while on the ZYNQ platform, we employed the FPDHFF.

According to Table III-C, it's evident that on the STM32 platform, a single harmonic analysis takes about 10.87ms, whereas employing the FPHDFF-based ZYNQ platform reduces this time drastically to just 0.33ms. This reflects a difference of approximately 33 times between the two platforms. FPHDFF fully leverages the parallel computing advantages of FPGA, thus significantly enhancing the speed of harmonic analysis.

VI. Conclusion

In this study, we proposed a fast power harmonic detection framework based on FPGA, which enhances the conventional FFT algorithm by incorporating interpolation calculations to effectively address the issue of non-coinciding harmonic frequencies on the spectral lines. This innovative tool is employed to identify harmonics within power networks. When addressing the task at hand - harmonic detection, FPDHFF exhibits impressive speed, far surpassing the performance of conventional MCU devices while maintaining commendable accuracy. The thrilling outcome emanating from this project ignites anticipation for future beneficial implementations where the FPDHFF can further prove its efficacy across diverse scenarios.

Acknowledgment

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